INTEGRATED LOW NOISE, LOW POWER AMPLIFIERS, AND CONTROL FOR THE RECORDING OF ELECTROCORTICOGRAMS

by

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SUPERVISORY COMMITTEE APPROVAL

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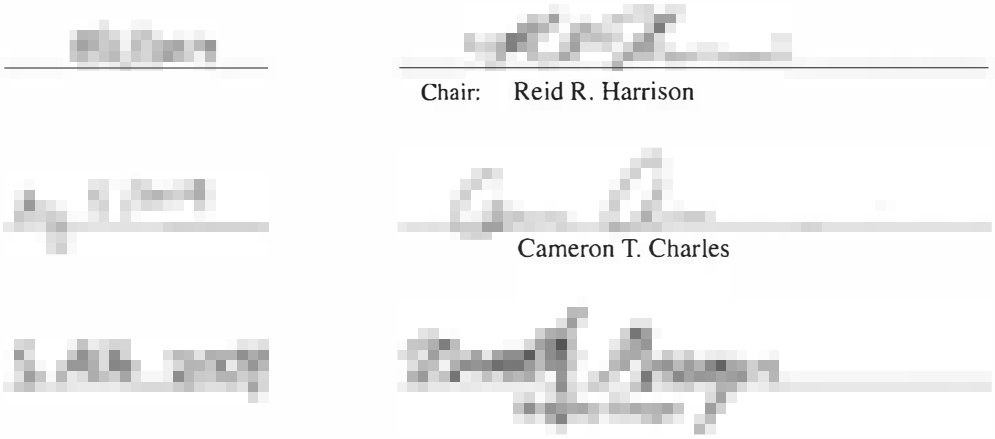

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ABSTRACT

Brain machine interfaces allow one to use one's thoughts to control the actions of a machine. To accomplish this, the interface must record and send brain signals to a signal processor to be decoded. The recording of brain signals such as the firing of individual nerves and electroencephalograms has been used for some time now to control machines. Recently it has been discovered that electrocorticograms are also a viable brain signal to control machines. This thesis covers the design and testing of the amplifiers and digital control for an integrated circuit that can record electrocorticograms and broadcast such data from multiple electrodes. The chip is powered wirelessly by an inductive link operating at 2.765 MHz. This same link uses amplitude modulation to send commands to the chip. Data can be collected from 100 electrodes. Each electrode is capacitively coupled to an amplifier. Each amplifier's output can be multiplexed to an ADC, digitized and then broadcast off chip via an RF transmitter. The chip was fabricated in a commercially available 0.6 μm, 2 poly, 3 metal BiCMOS process. The chip was tested, and all functions of the chip performed within their respective design tolerances. Specifically, the amplifier's bandwidth ranges from 0.05 Hz to a programmable high cut-off frequency of 79 Hz to 240 Hz. The amplifier has an electrode-referred noise of 3.5 μV and requires 4.5 μW of power. The transmission of data from multiple electrodes was also tested and it was found that individual electrode data could be reconstructed.

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CHAPTER 1

INTRODUCTION

Amputees may have lost an extremity, but that does not mean that the amputees' brain has lost the capability of producing signals that once controlled the extremity. If these brain signals were recorded and decoded into motion commands, the commands could then be sent to, and executed by, a prosthetic limb; effectively restoring, mobility, self reliance, freedom, and higher environmental control, to a patient. It is to this end that the following research and design of an integrated circuit that can record electrocorticographs, a type of brain signal, was conducted. The integrated circuit is called INI-E1.

1.1 Types of Electrical Brain Signals

Electrical brain signals originate from cells called neurons. One way neurons communicate with each other is by controlling ions that create a voltage, or action potential, that other neurons can sense. By placing an electrode next to a neuron it is possible to electrically sense, and record, the same voltage potential meant for other neurons. A recording of a neuron "firing" an action potential can be seen in Figure 1.1 [2].

Due to the nature of the brain, neurons in proximity to each other will often fire close in time to one another. If an electrode is placed some distance away from a cluster of neurons, the electrode will be able to electrically sense the combination of all the neural action potentials within the cluster. This combination of action potentials creates a type of brain signal called a local field potential, or LFP. These LFPs have different electrical characteristics than that of neural action potentials. For example, an LFP is a continuous time signal, unlike a neuron's discrete status of either firing or not.

Local field potentials can be recorded throughout the brain and even outside the brain. When electrodes are placed on the surface of the brain, either outside or just

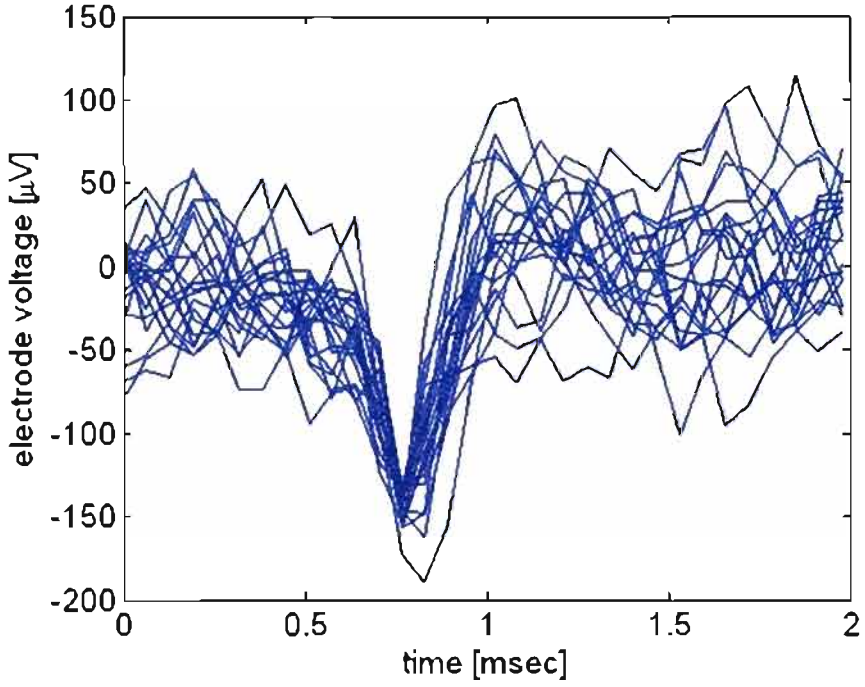

Figure 1.1. Electrode-referred neural signals recorded from auditory cortex of a cat using a Utah Electrode Array and transmitted wirelessly.

inside the dura-mater, the recording of LFPs is called electrocorticography, or ECoG (see Figure 1.2). When the electrodes are placed on the skin outside the skull, the recording of LFPs is called Electroencephalography, or EEG (see Figure 1.3). Due to the added attenuation of the skull EEGs have a smaller magnitude than that of ECoG. Also the higher frequencies of LFPs, usually those above 40Hz, are lost when recorded as an EEG. ECoG also has a tighter spatial resolution[1] than that of EEGs as the signals are not only truncated and attenuated by the skull, but also dispersed. These factors allow more information to be decoded from ECoG than from EEGs [3] (see Table 1.1).

1.2 Previous Work Done in Individual Neural Recording

Scientists and engineers at the University of Utah have created new technology that can record and transmit the firing of individual nerves within the brain [2]. This technol-

[1]The minimum distance that electrodes may be placed and pick up unique signals.

Table 1.1. Electrical characteristic comparison of EEG and ECoG signals

Electrical Characteristics	EEG	ECoG
Frequencies	$\leq$ 40Hz	$\leq$ 1000Hz
Voltage Magnitude	0.01-0.02 mV	0.05-1.0 mV
Spatial Resolution	3.0 cm	0.125 cm

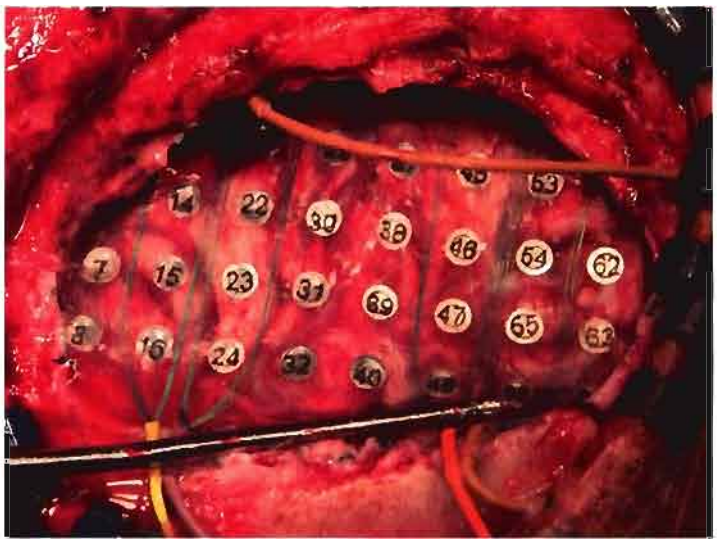

Figure 1.2. ECoG electrode array

ogy (Figure 1.4) can record from 100 electrodes and consists of a mixed-signal integrated circuit (INI-R1),[2] a Utah Electrode Array (UEA), micro-machined planar inductors, and two surface mount capacitors. Once packaged in bio-compatible material, the device can then be implanted into the brain. This technology is completely wireless. The recorded data are sent, wirelessly, out of the body by a RF transmitter on chip. The chip is powered through mutual inductance, wirelessly. Even the commands are given to the package, wirelessly, by amplitude modulation of the power. By having the technology wireless, complications due to the tethering effect of wires and an open wound, serving as a path for the wires to the brain, are avoided. This technology is fully capable of recording the electrical activity of individual neurons.

[2]Many revisions of this chip have been made since the publication of [2]

Figure 1.3. EEG electrode array

1.3 Previous and Ongoing Research in ECoG

1.3.1 Seizures

Traditionally ECoG signals were used almost exclusively for identifying seizures in patients. This is still the main reason ECoG recording is used, and the practice is still being researched [4, 5, 6]. In this application the brain activity of a patient having a seizure is recorded so as to localize the focus of the seizures. If the neurons are in an area of the brain that can be removed, then that part of the brain is removed, resulting in a high success rate of the patient not experiencing seizures again.

1.3.2 BCI's and Prosthetic Control

A brain computer interface (BCI) is a device that interfaces neural signals in the brain with a computer, such that the neural signals can control the computer. In turn, the computer can then be setup to control an object in the physical world. BCIs are currently being researched to control prosthetics, wheel chairs, and the cursor on computers. Within the last 5 years it has been found that motor control is encoded within ECoG signals. Leuthardt et al. were the first to use ECoG in a closed loop system to control a one-dimensional binary task [7]. Since then others have also explored the potential of using ECoG as a signal for BCIs [8].

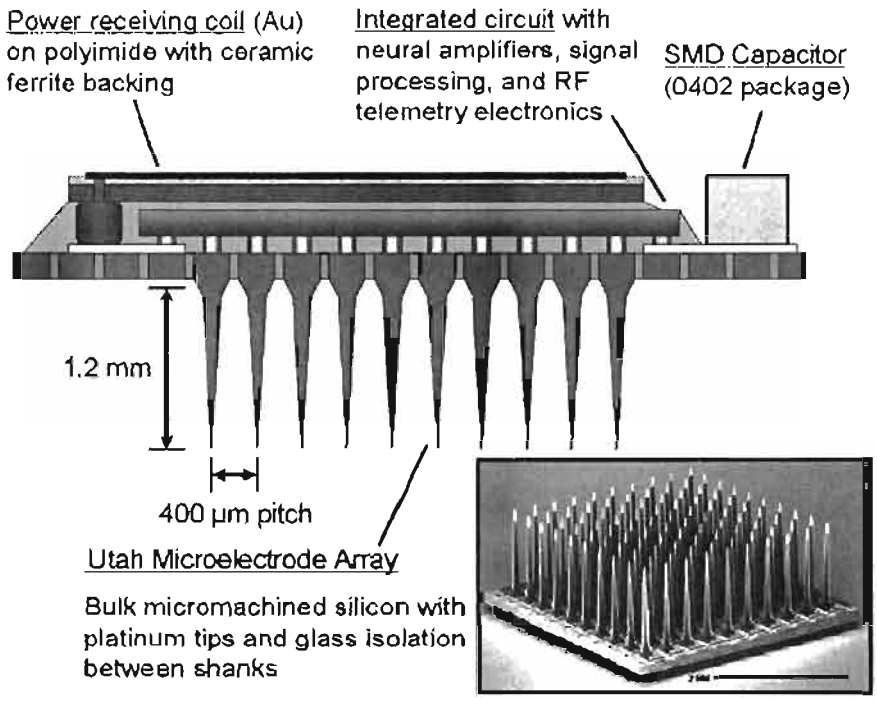

Figure 1.4. The concept of the wireless neural recorder

1.3.3 Recovering Speech

ECoG is also being used to study which areas of the brain are used in language processing [9]. Researchers in this area are also optimistic about connecting BCIs, recording from Broca's area[3] of the brain, to control a speech synthesizer. Thus, people who have lost the ability to speak, due to lack of motor control, have the opportunity to still communicate verbally.

1.4 A New Way to Record ECoG

The current method of recording ECoG is to place an array of electrodes on the brain, such as in Figure 1.2, and run the wires out of the brain to amplifiers. This method has a few disadvantages.

1. The tethering force of the wires requires the patient to stay somewhat immobile.

[3]Brocas area is associated with various language tasks

2. Long term, the site where the wires protrude is at high risk for infection.

3. Long wires are susceptible to pick up 60 Hz noise from AC power wires [8, 9, 10]. As 60 Hz is in the bandwidth of interest this interference can be detrimental to the integrity of the signal.

By modifying the current technology of the INIR integrated circuits, discussed in Section: 1.2, a viable solution for *wirelessly* recording ECoG signals has be developed.

Many of the challenges in designing a wireless ECoG recording IC are the same as for individual neuron recording. These challenges include

- Biocompatibility
- Low power dissipation
- Wireless power delivery
- Low electrode-referred noise

The solutions to some of these challenges are the same as for the INIRs [2]. The power regulator, command recovery circuitry, ADC and RF transmitter used on the INIRs were incorporated on INI-E1. Also the INIRs have a 10x10 array of pads that can be flip chip bonded to the 100 electrode UEA. The circuitry that supports each electrode is placed between the pitch of these pads. The pitch and pads of INI-E1 are the same as the INIRs.

However, due to the different nature of ECoG signals (Table 1.2), the design of INI-E1 required modification of some circuitry. INIRs were designed to record a neuron firing in terms of a voltage spike. Thus each electrode is connected to a threshold-based spike detector. When the voltage on the electrode exceeds the detectors threshold, information containing which electrode recorded the firing is sent off chip through the RF transmitter. ECoG information is not discrete like a neuron firing, but is a continuous analog signal, which allowed the peak detectors to be discarded.

The amplifiers needed to be modified to amplify ECoG signals. ECoG signals have amplitudes ranging from 0.05 mV to 1 mV and a frequency spectrum of sub hertz to 1000 Hz [11, 4, 3]. However, motor control signals are found primarily in the sub hertz

Table 1.2. Electrical design characteristic differences of individual neurons and ECoG recorders

Parameter	Individual Neurons	ECoG
Frequencies	300 Hz - 5 kHz	0.1 Hz - 200 Hz
Voltage Magnitude	30 V - 2mV	50 μV – 1 mV
Type of Signal	Discrete Signal	Continuous Signal

to 200 Hz range [3]. This is a narrower frequency spectrum than that for which the INIRs were designed to record, which allowed the amplifiers to be modified to have a smaller bandwidth, theoretically resulting in a lower input referred noise level.

In addition to modifying the amplifiers, new digital circuitry was added to facilitate getting the ECoG signals off chip. The purpose of the ADC on the INIRs is to be able to see the signal an individual electrode receives, then set the peak detector to the appropriate level for its signal. To change which electrode's output is sent to the ADC, a command is required from off chip. This micro-managing of which electrode's signal is sent to the ADC is undesirable for recording ECoG. Thus, the new digital circuitry is able to take commands and autonomously switch which electrode's signal is being sent to the ADC. For the ADC to sample the signals on the electrodes at speeds necessary not to lose data, the amplifiers connected to the electrodes were modified to enable faster multiplexing.

1.5 INI-E1

The culmination of the modifications is INI-E1 (Figure 1.5). INI-E1 is an integrated circuit with 100 bandpass amplifiers. Each of the 100 amplifiers can be bonded to an ECoG electrode. The pass band of the amplifiers is from sub hertz to a programmable high cutoff frequency. With the high cutoff frequency programed to 200Hz the input referred noise is well below 5μV. INI-E1 can either wirelessly transmit the data continuously from one of the electrodes, or it can be programmed to rotate through a circular pattern of 29 electrodes. These features will help neural researchers in decoding ECoG signals for seizures, prosthetics, speech, and many other BCIs.

Figure 1.5. Layout of INI-E1 (4,675 μm $\times$ 5,365 μm)

1.6 Preview of Upcoming Chapters

This thesis will take the reader through the design and testing of INI-E1. Chapter 2 will give an overview of the entire system. Chapter 3 will discuss the design of the amplifiers. Chapter 4 covers the design of the multiplexing logic. Chapter 5 will explain how to program the IC. Chapter 6 will discuss the characterization, testing, and other performance results of INI-E1. Chapter 7 will summarize and conclude the work, compare the amplifier to a similar amplifier, and make recommendations for continued work.

CHAPTER 2

SYSTEM OVERVIEW TO RECORD ECOG

The overall purpose of this project was to design a wireless system for recording ECoG that can be implanted into a patient's brain. This project is a continuation of research at the University of Utah to design wireless circuits for neural recording and stimulation [12, 13, 14]. While new amplifiers and circuitry for getting multiple signals digitized had to be designed, the solutions for wireless power and wireless transmission of information had already been proven in silicon from previous research. These circuit solutions did not need to be redesigned for INI-E1 and were used to accomplish those two tasks. This chapter will give an overview, in some detail, of the entire INI-E1 chip. It begins with a system-level view of the chip. Then the circuits used from previous research will be explained, followed by a brief discussion of how they integrate with the new amplifiers and control circuity, whose design is detailed in later chapters.

2.1 System-level View

To accomplish wireless recording of electrocorticograms, the following circuit blocks are needed:

- Power rectifier and regulator
- Clock generator
- Incoming data recovery
- Radio frequency transmitter
- ADC to digitize data for transmission
- Amplifiers

- Sensors that monitor the state of INI-E1
- Control circuitry to support the digitization of multiple electrode signals
- Memory cells to store control information for various blocks

Combined these blocks form INI-E1 which is capable of recording electrocorticograms from 100 electrodes and continuously transmitting the data from 29 of them. The block diagram of INI-E1 is shown in Figure 2.1.

The chip is powered wirelessly through mutual inductance [15]. The inductor and capacitor, for the wireless power transfer, are shown in Figure 2.1 even though these are off chip. The power produced by this resonant circuit is then rectified. The rectified power is then regulated to keep a constant voltage for all the circuits on the chip.

A clock is required to synchronize operations throughout the chip. However, to limit the number of off chip components required to operate INI-E1, there is no crystal oscillator. The system clock is recovered from the inductive link, and is based off of the frequency of the transmitted power.

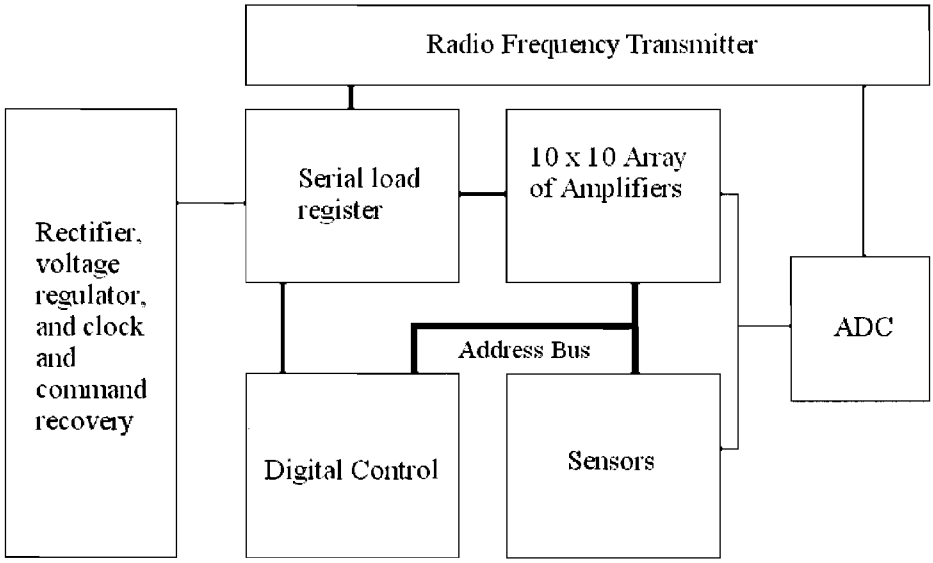

Figure 2.1. The block diagram of INI-E1

The inductive link is also the means by which commands are sent to the chip via amplitude-shift-keying (ASK). When no commands are being sent to the chip, the voltage across the transmitting coil is at a constant value that can power the chip. To send a bit of information the voltage across the transmitting coil is increased, which also increases the voltage seen across the receiving coil. This increase is sensed, on chip, by a data recovery circuit. The data recovery circuit is able to interpret the modulation of the power according to the ASK scheme. If a valid command is sent to the chip the data recovery circuit will execute it.

A radio frequency transmitter is on chip to wireless radiate the data acquired by INI-E1. The RF transmitter uses a digital frequency-shift-keying (FSK) scheme to transmit its data. As the data being recorded by the chip is analog, an ADC is needed to digitize the analog signals. Once the data are digitized they are then transmitted off chip.

To amplify the ECoG signals there is a 10×10 array of amplifiers (see Figure 2.2). Each amplifier is made up of three stages. There are three programmable bias generators on chip. Each bias generator produces a dc bias current for one of the three stages. To minimize power, all 100 instances of the individual stages are biased from the same bias generator.

There are two sensors on chip: a temperature sensor and an unregulated voltage sensor. These sensors' output can be sent to the ADC to monitor the status of the chip.

To facilitate the transmission of signals from multiple electrodes, there is a block of digital logic that can control what data are sent to the ADC for transmission.

Many of the above circuits behavior and electrical characteristics are controlled by commands from off chip. A single, serial-loaded register is used as memory and contains the most recent commands sent. The register is programed through the data recovery circuit. This register can be sub divided and thought of as different registers. Each smaller register contains a subset of bits of the actual register. These registers control the amplifiers bias, the frequency and transmission power of the RF transmitter, and the address bus.

Figure 2.2. The 10×10 array of amplifiers and the address bus.

2.2 Capability of Previously Designed Blocks

Some of the circuits that make up INI-E1 were designed previously for other neural applications. The capabilities of the previously designed circuits need to be known to understand some of the design requirements for the custom circuitry used on INI-E1. The previously designed circuits and their applicable specifications are:

- The power rectifier needs to receive enough power so that the rectified voltage is at least 1 V above the regulated voltage.
- The regulator will supply a regulated voltage of 3 V.

- The clock generator produces a square wave whose frequency is 15.7 kHz.
- The incoming data recovery is triggered by a voltage increase of 25% above baseline. It is capable of 20 kbit/s data reception.
- The radio frequency transmitter is designed to operate in the 902 – 928 MHz bandwidth. The two frequencies it switches between, for the FSK, are separated by 600 kHz.
- The ADC samples the analog data at 15.7 kHz, has a linear range of 0 – 2 V and digitizes each sample into 10 bits.
- The unregulated voltage sensor reports one fourth of the unregulated voltage is. The temperature sensor has a resolution of 6 mV/°C.

2.3 Connecting the New and the Old

The outputs of all 100 amplifiers are connected to the ADC via an analog transmission gate. Only one transmission gate is transparent at any given time to ensure that only one signal is sent to the ADC at a time. The transmission gates are controlled by an address bus. The address bus is driven by eight of the bits in the serial register. Four of the eight bits represent a row number (0 – 9) in the 10×10 array and the other four represent a column number (0 – 9). When the bits in the register contain an address whose row and column numbers are within the 10×10 array, that electrode's amplified signal is then routed to the ADC. If the data in the address registers are not representative of an address in the 10×10 array, then one of four things happen:

1. The ADC input is not driven
2. One of the two on chip sensors output is driving the ADC input.
3. The digital control block is enabled and drives the address bus.
4. The input to the ADC is grounded.

Each sensors output, like the amplifiers, is connected to the ADC via an analog transmission gate. However, unlike the amplifiers transmission gates, the transparency of the sensors transmission gates is controlled only by the 4 bit row address register. Each sensor has a unique row address whose value is not within the range of the 10×10 array.

To enable the digital control logic the row address is programmed to a unique value that is not the address for one of the sensors, nor is it in the range of the 10×10 array. The control logic contains five different patterns, each containing 32 different addresses of electrodes and sensors. When enabled, the control logic will drive the address bus and cycle through one of the address patterns. At every clock cycle, the control logic will switch which electrode, or sensor output is driving the ADC. The value of the column address register determines which pattern is cycled through.

If the row address register contains a value that is not in the range of the 10×10 array, does not correspond to a sensor, and does not engage the digital control logic, then no transmission gates will be transparent and nothing will be driving the ADC.

By integrating the newly designed amplifier and control circuitry, with the already proven wireless power and wireless data transmission, a viable solution to record ECoG has been developed. These systems combined formed the integrated circuit INI-E1.

CHAPTER 3

AMPLIFIER DESIGN

The amplitude of the ECoG signals directly sensed by the electrodes is too small for the ADC to digitize directly. Thus before the signals are sent to the ADC, they must first be amplified. This chapter goes over the design process for the amplifiers. It begins by explaining the specifications for the amplifiers. The chapter then sets forth the overall design of the amplifier. Then the individual stages of the amplifiers are discussed. The chapter concludes with the verification that the design meets the specifications.

3.1 The Specifications for the Amplifier

The specifications for the amplifier are set by the nature of the ECoG signals and the limitations of the hardware used to record them. The specifications are justified below and summarized in Table 3.1.

First, the amplifier must fit in the spacing between electrodes. The electrodes will have a pitch of 400 μm in both directions; this is done to keep a consistency in the electrode pitch of the previously done research, of neural recording and stimulation, that has been done with the same grant money. The electrode takes up a little less than 13,500 μm^2, leaving 146,500 μm^2 for the amplifier to fill.

Table 3.1. Specifications for the amplifier

Electrical Specification	**Value**
Low Cut-off Frequency	$\leq$ 0.1 Hz
High Cut-off Frequency	$\geq$ 200 Hz (programmable)
Gain	60 dB
Power Consumption	$\leq$ 20 μW
Slew Rate	$\geq$ 1 V/μs
Layout Area	$\leq$ 146,500 μm^2
Input Referred Noise	$\leq$ 5 μV_{rms}

Referring back to Table 1.2 the amplitudes of ECoG signals range from 50 μV to 1 mV. The ADC's linear input range is 0-2 V. Thus the amplifier should be designed to have a reference voltage of 1 V and an amplification of 1,000 V/V or 60 dB. This would allow the largest raw signal, of 1 mV, to be amplified to an amplitude of 1 V and still be fully represented in the linear region of the ADC.

So as not to degrade the incoming signal, the noise produced by the amplifier should not exceeded 10% of the amplitude of the smallest input voltage. Thus the input refered noise voltage should be less than 5 μV.

While the amplifier has to be low noise it also has to be low power. The more power the circuit draws the more the circuit will heat up and over heat brain cells, causing them to die. If each amplifier drew 20 μW or less then combined, the 100 amplifiers would only use 2 mW, which would be acceptable.

The bandwidth of the amplifier should mimic the bandwidth of the signal, and thus should be from 0.1-200 Hz. However, not all applications of recording ECoG signals require the high cut-off frequency to be as high as 200 Hz. Lowering the high cut-off frequency of the amplifier will also lower the input referred noise of the amplifier, and thus it makes sense to have the high cut-off frequency programmable.

Finally, when the IC is in a state of multiplexing through the electrodes, each electrode's signal is sent to the ADC for 63.66 μs. Thus to ensure that the line to the ADC settle's within 5% of the period, a slew rate of 1 V/μs is needed.

3.2 The Architecture of the Amplifier

A DC offset in the brain tissue, that the electrodes are placed in, contains no information and could cause the amplifiers to saturate. Capacitively coupling the electrodes to the amplifiers blocks the DC offset. However, the blocking capacitor will also block low frequency signals. To prevent the blocking of desired low frequencies, the architecture in Figure 3.1 is used [16, 17]. As will be shown, this design allows all the specifications to be met.

To find the transfer function of the architecture, replace the amplifier in Figure 3.1 with an ideal voltage controlled current source as seen in Figure 3.2. Then using basic straightforward circuit analysis, it can be found that the transfer function is:

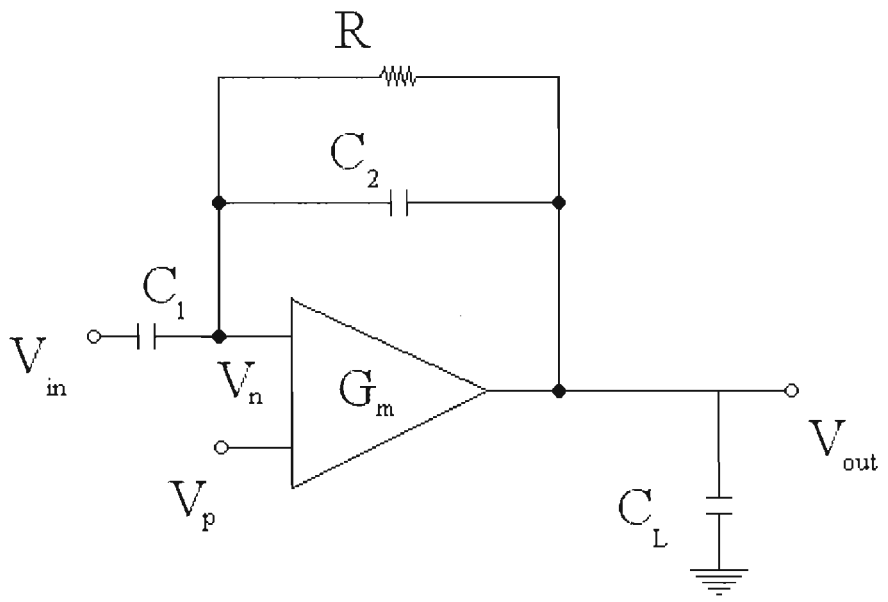

Figure 3.1. The amplifier's architecture

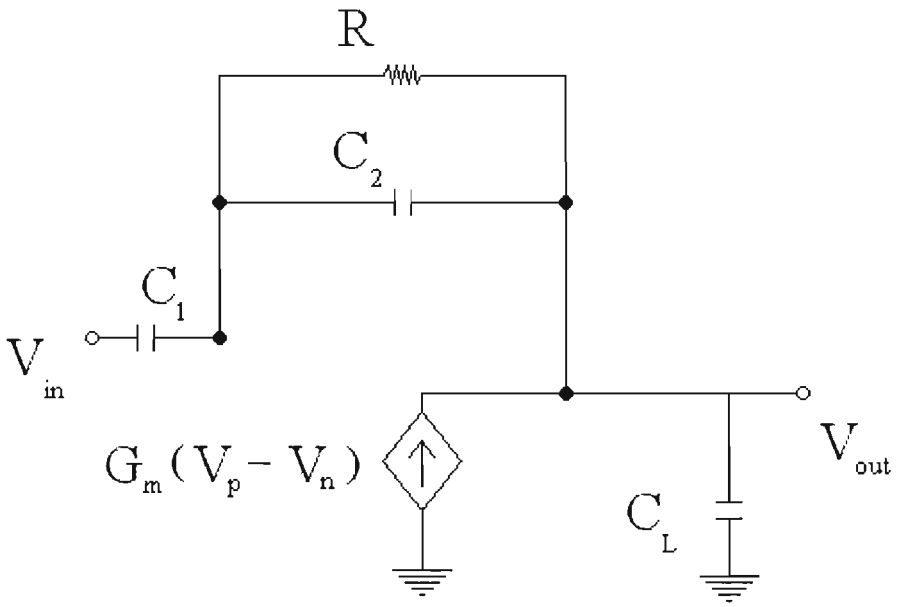

Figure 3.2. Schematic used to determine the transferfunction.

$$\frac{V_{Out}(s)}{V_{In}(s)} = H(s) = \frac{-\frac{C_1}{C_2}s\left(1 - s\frac{C_2}{G_m}\right)}{s^2\left(\frac{C_L}{G_m} + \frac{C_1}{G_m} + \frac{C_L C_1}{G_m C_2}\right) + s\left(1 + \frac{C_L}{C_2 R G_m} + \frac{C_1}{C_2 R G_m}\right) + \frac{1}{C_2 R}} \tag{3.1}$$

Making the assumptions that:

$$\frac{1}{RC_2} \sim 1 \text{ Rad/s} \tag{3.2}$$

$$C_2 << C_1 \tag{3.3}$$

$$C_2 << C_L \tag{3.4}$$

the transfer function becomes:

$$H(s) = \frac{-\frac{C_1}{C_2}s\left(1 - s\frac{C_2}{G_m}\right)}{s^2\frac{C_L C_1}{G_m C_2} + s + \frac{1}{C_2 R}} \tag{3.5}$$

The denominator of (3.5) is a simple quadratic of type $as^2 + bs + c$. To approximate the roots of a quadratic define: $F = \frac{1}{2} + \frac{1}{2}\sqrt{1 - 4Q^2}$ where $Q^2 = ac/b^2$. The roots are then:

$$r_1 = -\frac{b}{a}F \qquad \text{and} \qquad r_2 = -\frac{c}{b}\frac{1}{F} \tag{3.6}$$

which simplify to the classic quadratic equation. Looking at the above definitions for F and Q^2, as $Q^2 \to 0$, which is true with the assumptions already made, then $F \to 1$. This means that our roots will simplify to:

$$r_1 = -\frac{b}{a} \qquad \text{and} \qquad r_2 = -\frac{c}{b} \tag{3.7}$$

Applying these roots to the amplifier's transfer function (3.5) and moving the zero, at zero, down to the denominator to make an inverted pole, it follows that the transfer function can be simplified to:

$$H(s) = \frac{-\frac{C_1}{C_2}\left(1 - s\frac{C_2}{G_m}\right)}{\left(\frac{\frac{1}{C_2 R}}{s} + 1\right)\left(\frac{s}{\frac{G_m C_2}{C_L C_1}} + 1\right)} \tag{3.8}$$

Or:

$$H(s) = A_M \frac{\left(1 - \frac{s}{2\pi f_Z}\right)}{\left(\frac{2\pi f_L}{s} + 1\right)\left(\frac{s}{2\pi f_H} + 1\right)} \tag{3.9}$$

where:

$$\text{The midband gain} \qquad A_M = -\frac{C_1}{C_2} \tag{3.10}$$

$$\text{The low cut-off frequency} \qquad f_L = \frac{1}{2\pi C_2 R} \tag{3.11}$$

$$\text{The high cut-off frequency} \qquad f_H = \frac{G_m C_2}{2\pi C_L C_1} = \frac{G_m}{2\pi C_L |A_M|} \tag{3.12}$$

$$\text{The zero frequency} \qquad f_Z = \frac{G_m}{2\pi C_2} = f_H \frac{C_1 C_L}{{C_2}^2} \tag{3.13}$$

Equations (3.10) - (3.13) show that each parameter of the transfer function (3.9), seen in Figure 3.3, can be set independently of each other. The zero can be set by C_2. The midband gain is set by the ratio $\frac{C_1}{C_2}$. The low cut-off frequency can then be chosen by R. Finally, choose C_L to set the high cut-off frequency.

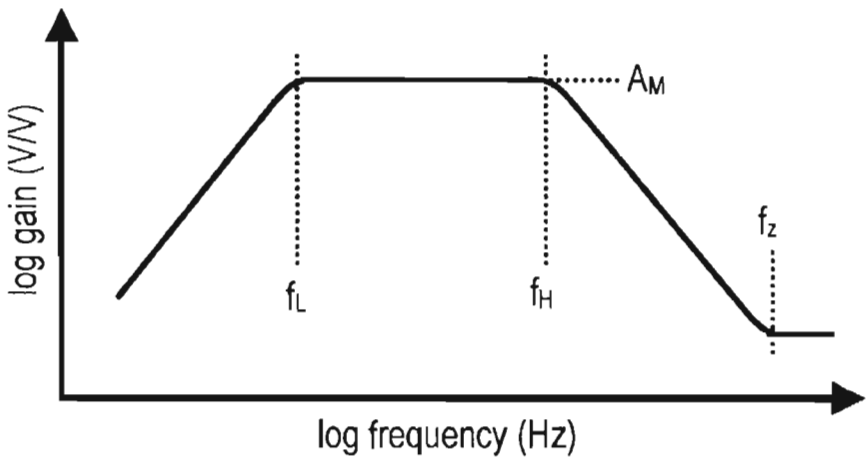

Figure 3.3. The magnitude bode plot of equation (3.9)

This analysis holds only if assumptions (3.2) – (3.4) are valid. To show that these assumptions are valid take C_2 to be 0.2 pF then to get a gain of 100 C_1 would have to be 20 pF. This validates assumption (3.3). C_L can be chosen to validate assumption (3.4). To satisfy assumption (3.2) requires R to be in the Teraohms. However, this is possible by using diodes as the resistive elements in Figure 3.1 as suggested in [16].

With the assumptions validated, the amplifier can be designed by using the design equations: (3.10) – (3.13). Equation (3.10) shows that the gain is the ratio C_1/C_2. To get a gain of 60 dB, C_1 must have 1000 times the capacitance of C_2. To limit the percentage of parasitic capacitance making up C_2, so as to control the absolute value of C_2, C_2 must be on the order of 100 fF. This would mean C_1 would be on the order of 100 μF which would be too large for an on chip capacitance. Thus to get the gain required, two amplifying stages must be used. Dividing the gain into one gain stage of 40 dB and one of 20 dB will allow reasonable capacitor sizes for C_1 and C_2 on each gain stage.

To minimize noise, the first gain stage will be the 40 dB. The noise can be further reduced by having each stage have the same bandwidth. By the gain stages having the same bandwidth the overall transfer function of the amplifier will have a -40 dB/decade slope at each cut-off frequency, thus reducing the amplification of out-of-band noise.

The slew rate specification for the amplifier is for the worst case scenario when the input to the ADC is switched from an amplifier whose output is at 0 V to an amplifiers whose output is 2 V. As the load of the ADC on the amplifier is generally capacitive, the slew rate can be modeled as:

$$I = C\frac{dV_c}{dt} \tag{3.14}$$

where I is the current supplied by the amplifier, C is the capacitive load on the amplifier and dV_c/dt is the slew rate. Thus to achieve a high slew rate requires the output stage of the amplifier to have a high current. The slew rate needed for a sinusoid of amplitude A and frequency ω in radians/s, is:

$$\frac{dV_c}{dt} = A\omega \tag{3.15}$$

This means that under normal operation the amplifier only needs to have a slew rate of 1.26 mV/μs. As shown in the specifications the worst case scenario requires a slew rate of 1V/μs, almost 1000 times that of normal operation. For a given capacitance this would require the amplifier to produce 1000 times the amount of current for the worse case scenario than for the normal operation. To always be drawing the amount of current needed to satisfy the worse case scenario is a waste of power as the scenario will rarely happen. To conserve power the final stage of the amplifier is a buffer made from an OTA with some positive feedback to make it draw more current when it slews [18]. By only drawing high current when slewing the amplifier will use less power.

3.3 Stages 1 and 2: The Gain Stages

The amplifier's first two stages are to provide a total of 60 dB of gain. To minimize noise requires more gain in the first stage. However, as the gain increases in the first stage the size of C_1 also increases. Thus there is a trade off between low noise and area in choosing the gain for the stages. As there are other ways of decreasing the noise, the gain of each stage was chosen so that the capacitors of each stage would have reasonable values. The first stage provides 40 dB of gain and the second stage supplements the remaining 20 dB.

The op-amps for stages 1 and 2 need to have low offset voltages and low power. As they drive capacitive loads, current mirror op-amps were chosen as the amplifiers for stages 1 and 2 [19]. Figure 3.4 shows the schematic for the op-amps used in stages 1 and 2. Though the architecture for the opamps are the same, the sizing of the transistors are different for each stage. Their sizings can be seen in Table 3.2.

Table 3.2. Transistor sizes for stages 1 and 2

Transistor	Ratio for Stage 1	Ratio for Stage 2
M1, M2	$8(\frac{100}{1.2})$	$2(\frac{10}{1})$
M3 – M6	$2(\frac{12.5}{50})$	$\frac{6}{12}$
M7, M8	$2(\frac{6}{6})$	$\frac{12}{6}$
M9	$\frac{16.2}{4}$	$\frac{16.2}{4}$

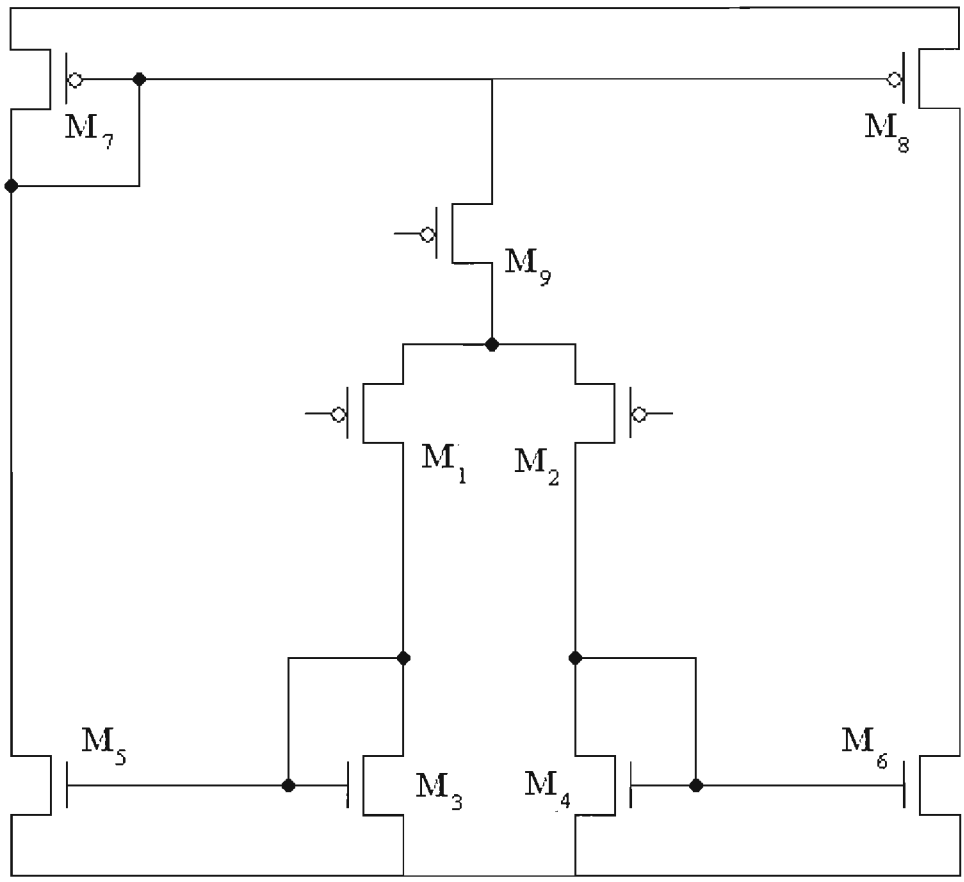

Figure 3.4. Schematic of stages 1 and 2

The transistors for stage 1 are larger than those for stage 2. This is to reduce the flicker, or $1/f$, noise. Flicker noise in a MOSFET can be modeled as:

$$V_g^2(f) = \frac{K}{WLC_{ox}f} \tag{3.16}$$

where V_g^2 is a voltage source in series with the gate of a MOSFET, K is a process and device dependent constant, W and L are the width and length of the transistor, and C_{ox} is the gate capacitance per unit area. As the flicker noise is inversely proportional to the area of the gate, $W \cdot L$, there will be less flicker noise for larger transistors. The transistors in stage 2 do not need to be as large as stage 1 because the signal will have already experienced 40 dB of gain from stage 1 so the signal to noise ratio will be higher.

Another way to look at is to realize that any noise added in the second stage will be divided by the gain of 100, from the first stage, to be input referred. This allows the transistors in the second stage to be smaller, saving area, while still keeping their input referred noise within specification.

Instead of sizing the transistors extremely wide to get the large gate area, the area was increased substantially in the first stage by increasing the length of the output transistors. This was done as the head room for the output is quite small and making longer transistors will increase the output impedance of the op-amp, making it a better transconductor. The output nMOS transistors for the second stage are wider than the first as their headroom needs to be increased. However, the output pMOS transistors, for the second stage, width to length ratio is the same as the first stage. This is fine as the V_{eff} for the transistor does not need to be less than 1 V.

The differential pair for each gain stage needs to have high transconductance. A MOSFET's transconductance is highest when it is operating in weak inversion [20]. In weak inversion the transconductance is given by:

$$g_m = \frac{\kappa I_D}{U_T} \tag{3.17}$$

where U_T is the thermal voltage, I_D is the drain current and κ is the sub-threshold gate coupling coefficient. It is easiest to size transistors to operate in weak inversion by having a transistors moderate inversion characteristic current [21], to be at least 10 times that of its drain current. The moderate inversion characteristic current, I_S is defined as:

$$I_S = \frac{2\mu C'_{ox} {U_T}^2}{\kappa} \frac{W}{L} \tag{3.18}$$

As long as

$$I_S \geq 10 I_D \tag{3.19}$$

then the transistor will operate in weak inversion and the transconductance will be maximized for a given bias current. This allows the amplifiers to have high transconductance at the price of area, instead of power, helping keep the circuit low power.

In addition to having the differential pair operate in weak inversion, power can be saved in the bias current to each amplifier. The bias current to each stage of the amplifier is set by a programmable bias network. Commands from off chip control the voltage on the nMOS switches that change the resistance seen by the bias circuit shown in Figure 3.5. The variable resistance controls the amount of current running through the transistors. This circuit does require a start up circuit that is not shown. Lowering the bias current does save power, but it also affects the transconductance of the differential input to the amplifiers. This in turn changes the high cut-off frequency as shown in equation (3.12). Therefore if the amplifier does not require the bandwidth that the maximum bias current provides, then the current can be tuned to give the bandwidth

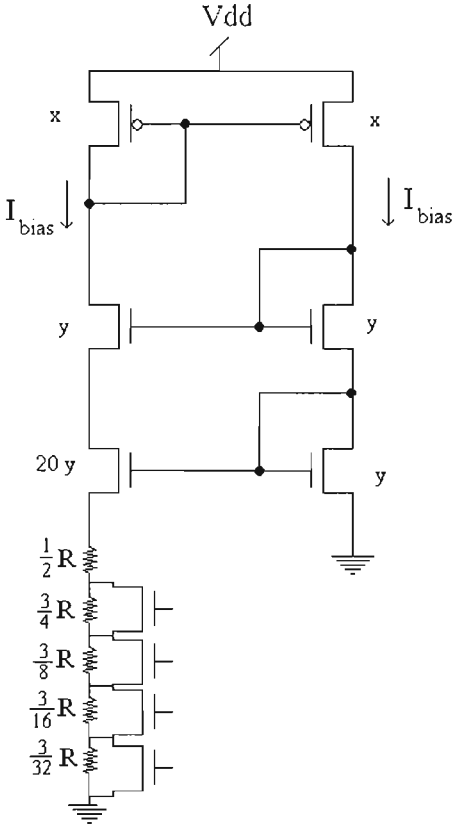

Figure 3.5. The bias generator for the opamps in stages 1 and 2 and the buffer. The required start up circuit is not shown. X and Y are transistor sizes.

needed for a given application. This will save power as well as decrease the input referred noise, as mentioned above. There are three bias generators on the IC, one for each gain stage and one for the buffer.

3.4 Stage 3: The Buffer

As explained at the end of section 3.2 the amplifier needs to be fast enough for the worse case scenario in which the amplifier has to change the ADC's input from 0 to 2 V, or visa versa. The specifications state that to do this the slew rate of the amplifier has to be 1 V/μs. The second gain stage of the amplifier is able to perform it's amplification within the specified bandwidth with a bias current of 10 nA. This allows a maximum of 10 nA of current to be produced at the output. Using the fabrications process specifications it was estimated that the input capacitance to the ADC was 3 pF. Using equation (3.14) the slew rate capable from the second stage, if connected directly to the ADC, would be 3.34 mV/μs. To achieve a slew rate of 1 V/μs on the 3 pF load would require at least 3 μA. To avoid this much static power consumption a buffer made from an adaptive biasing amplifier is used [18]. The adaptive biasing amplifier schematic is shown in Figure 3.6 and its sizes are shown in Table 3.3.

At its heart the adaptive biasing amplifier is a current mirror opamp, like the ones used for the gain stages. Added to the opamp are two current subtractors. The current subtractors subtract the current through the branches of the differential pair as shown

Table 3.3. Transistor sizes for stage three

Transistor	Ratio for Stage 3
M1, M2	$2(\frac{10}{0.6})$
M3 – M6	$\frac{6}{1.2}$
M7, M8	$\frac{12}{1.2}$
M9	$\frac{16.2}{4}$
M10 – M13	$\frac{6}{1.2}$
M14 – M19	$2(\frac{8.1}{4})$
M20 – M21	$4(\frac{8.1}{4})$

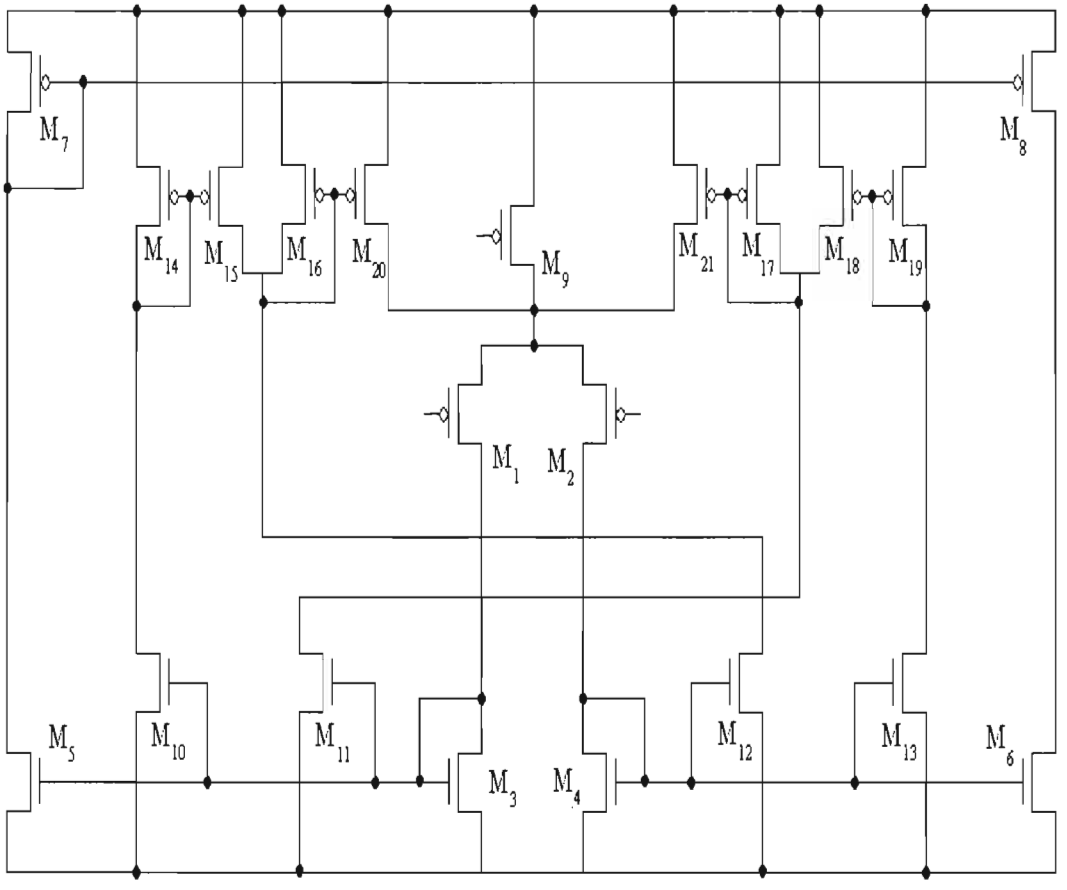

Figure 3.6. Schematic of stage three

below:

$$I_{D21} = m(I_{D1} - I_{D2}) \tag{3.20}$$

$$I_{D20} = m(I_{D2} - I_{D1}) \tag{3.21}$$

where m is the ratio of the width to length ratio of transistors M21/M17 and M20/M16. I_{D21} and I_{D20} are then fed to the source of the differential pair effectively increasing the bias current. Only when there is a difference between the drain currents in the differential pair will there be an increase in bias current. There will be a difference in the differential pairs current only when the opamp's output is not great enough to keep the differential pairs voltages the same. Thus the opamp will use more power only when it needs to be

faster than its quiescent current will allow it to be. This architecture allows the given slew rate to be met, while limiting the static power dissipated.

3.5 Simulation Verification of Specifications

The three stages previously discussed combine as shown in Figure 3.7. The diode connected transistors form the large resistance required for the amplifiers to work. Before the design was realized in layout it was simulated in a spice program to verify that it met the specifications.

Both gain stages and the buffer were simulated to test for stability. The phase margin for the first stage was found to be 56° for a β of 1, and 96° for a β of 1/100. The phase margin for the second stage was found to be 92° for a β of 1, and 137° for a β of 1/10. The phase margin for the buffer was found to be 88° for a β of 1.

The simulated transfer function is Figure 3.8. From the figure it can be verified that the gain and the bandwidth is within specification. The input referred noise summation, as a function of the bandwidth, is shown in Figure 3.9 and is well below the 5 μV specification.

To verify the slew rate a simulation was performed that had two buffers. One buffer's input was tied to ground, the other to a 2 V source. Their outputs were tied to a transmission gate, one that was transparent when its control was low, and the other, transparent when its control was high. The transmission gates were then connected to a 3 pF load, and their controls tied together. Figure 3.10 shows that both the rise and fall

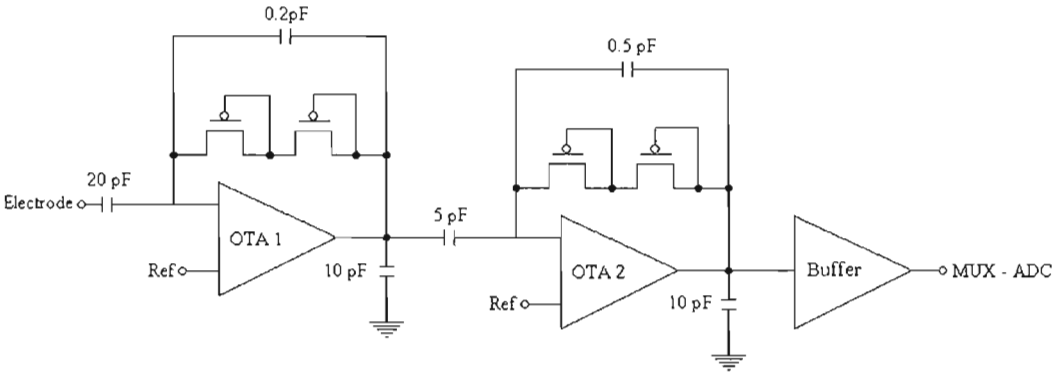

Figure 3.7. The three stages making the amplifier

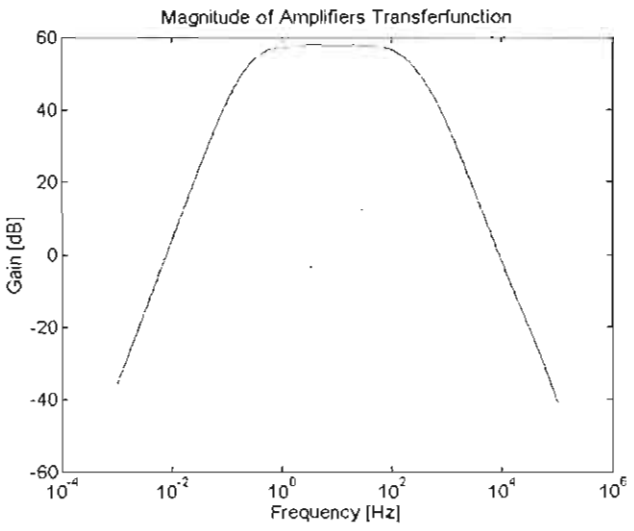

Figure 3.8. The simulated amplifier gain-frequency response

slew rates meet the 1 V/μs specification.

To find the power consumption of the amplifier a DC simulation was ran to find the current drawn from a 3 V power supply only connected to the amplifier. The amplifier drew 1.5 μA. With a 3 V supply this means that the amp uses 4.5 μW of power. This is well below the specification.

With all the electrical specifications met the layout of the design was produced and, as can be seen from Figure 3.11, was able to fit nicely in the amount of area between electrodes which is marked by the white border around the entire cell.

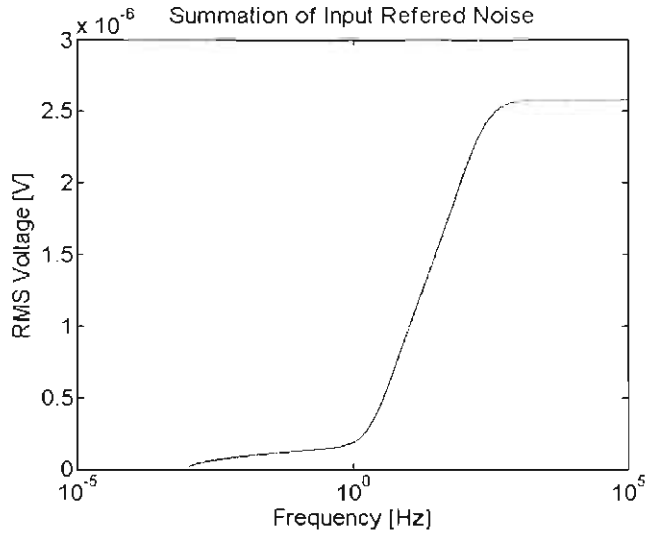

Figure 3.9. The input referred noise summation

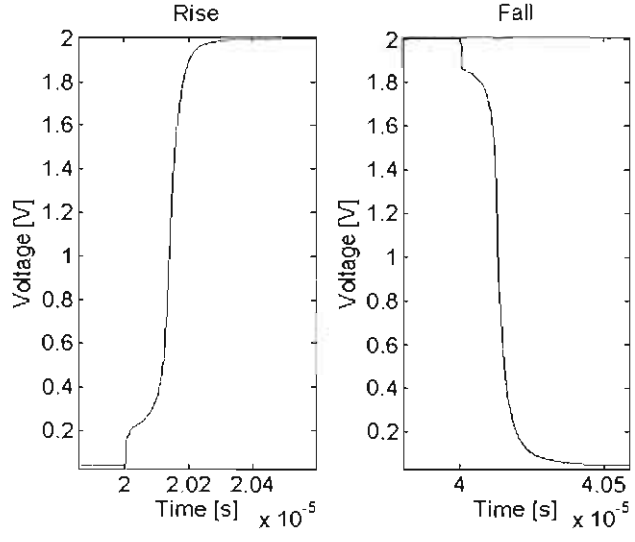

Figure 3.10. The positive and negative slewrates of the buffer

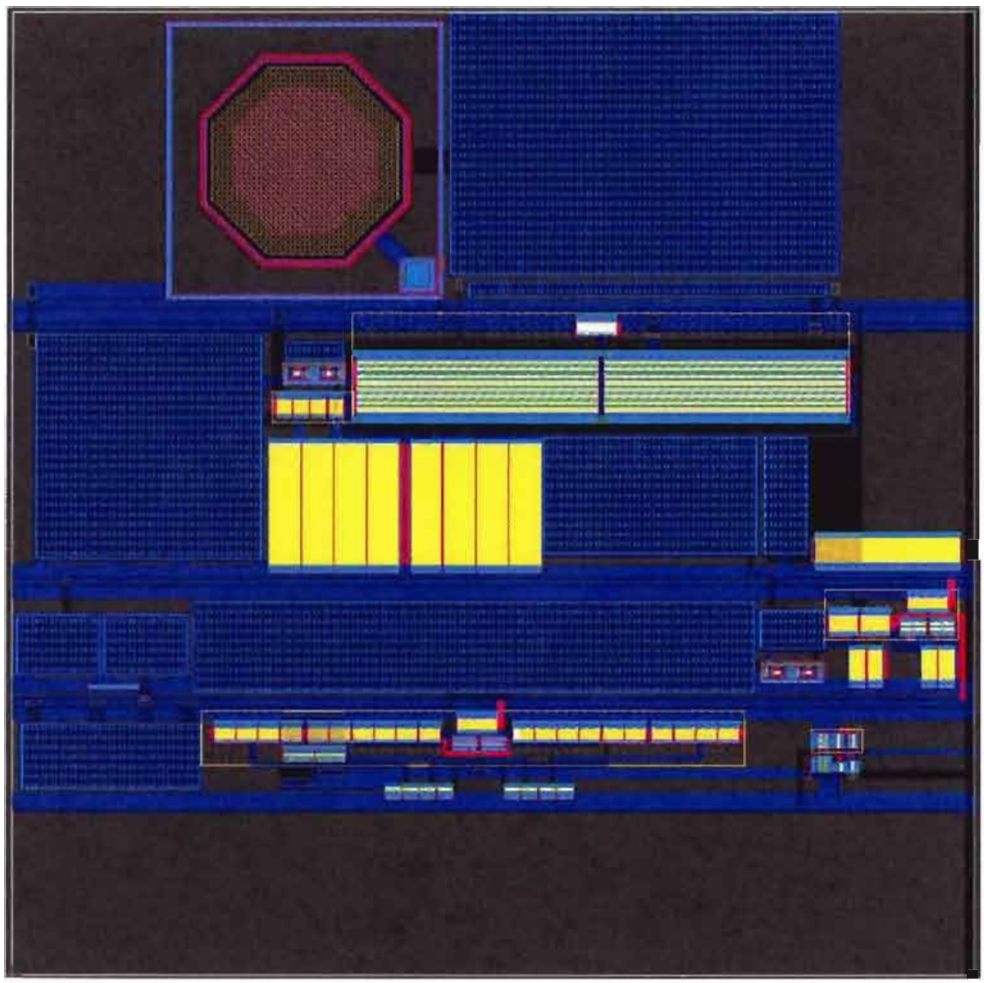

Figure 3.11. The layout of the three stage amplifier (400 μm $\times$ 400 μm)

CHAPTER 4

THE DIGITAL CONTROL

To transmit data off the integrated circuit an analog-to-digital converter (ADC) is connected to a radio frequency transmitter. To send multiple ECoG signals off chip, a digital control unit was designed to multiplex electrodes through to the ADC. This is possible because the ADC samples significantly faster than the ECoG frequencies, allowing each electrode's signal to be sampled above the Nyquist rate.

4.1 Nyquist Rate and Theory

As there is only one ADC on the chip connected to the radio frequency transmitter, only data from this ADC can be transmitted off chip. The ADC samples at approximately 16 kHz, so according to the Nyquist sampling theorem, this would allow the ADC to represent a signal whose frequencies do not exceed 8 kHz. At the same time the ADC could digitize multiple signals, as long as each signal is sampled at double its fastest frequency. As each amplifier signal extends no higher than 200 Hz, this would allow 32 electrodes to be sampled well within the Nyquist rate for each signal. (The 16 kHz sampling rate could allow 40 electrodes to be sampled, but, as digital logic is going to be used to realize the interface, it is easier to keep the number of electrodes being sampled to a power of two.)

4.2 Implementation

To implement the above mentioned scheme, a digital logic block is placed between the registers, that holds the value of the column and row addresses, and the address lines. When the registers hold a valid electrode address, or the address for one of the three sensor elements on chip, then that address will be directly routed to the address lines. If the row register holds a special address then the digital block will cycle through a subset

of the 100-electrode array. There are five different pre-programmed patterns that can be cycled through. Each subset pattern contains 29 electrodes and the three sensor elements. The five subsets are controlled by the column address (see Figure 4.1).

The logic is made up of four basic logic blocks that are connected as shown in Figure 4.2.

1. A multiplexer.
2. Select logic to control the multiplexer.
3. A five bit counter.
4. State logic.

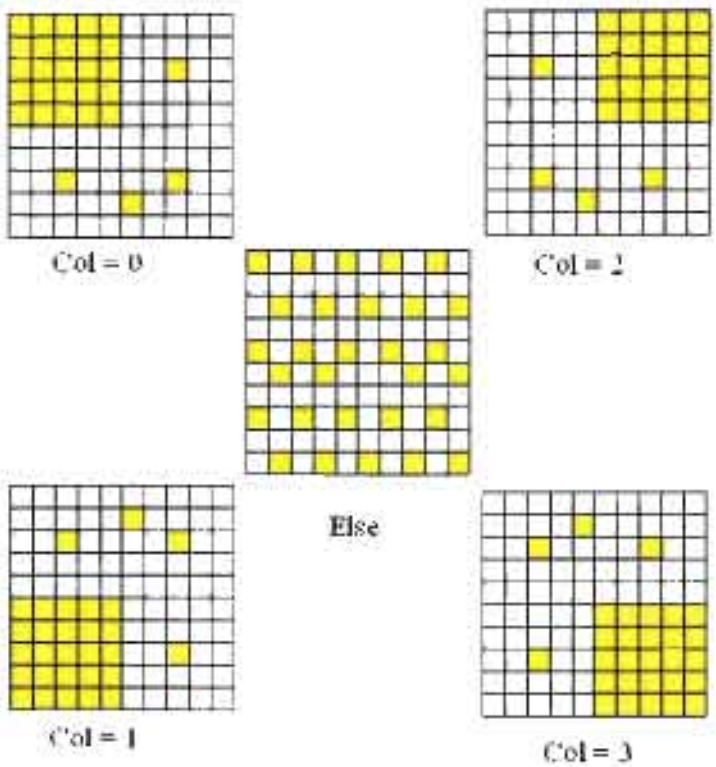

Figure 4.1. The five subsets. Each subset corresponds to the column address beneath it. The middle subset is the subset which is cycled through if one of the other four is not specifically chosen. Each 10 × 10 array is representative of the electrode array as viewed by orientating the RF transmitter at the top of the die.

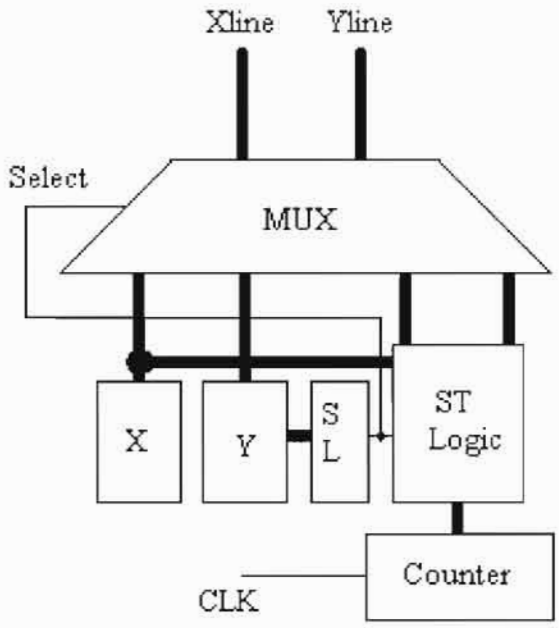

Figure 4.2. Block diagram of the digital control

If the row register (Y) has a value of 12, the select logic will enable the multiplexer to route the addresses from the state logic onto the address lines. If the row register contains any other value the select logic will have the multiplexer route the row (Y) and column (X) registers onto the address line.

The counter takes one input, the clock signal. At each positive edge of the clock the counter increments to the next number. It is continually counting from 0 to 31. The output from the counter is the value of the count at any given moment. This number serves to be a state register for the state logic.

The state logic is enabled by the select logic, like the multiplexer, when the row register has a value of 12. This is done to save power by preventing unnecessary switching of the state logic, when its output is ignored by the multiplexer. The state logic looks at the state of the counter and the column register to determine which ordered pair address it sends to the multiplexer. If the column register is not set to one of the decimal values

0 – 3 then the default rotation is cycled through. Table 4.1 shows which address is given based upon the state of the column register and counter. The address numbers correspond to the shaded boxes in Figure 4.1.

4.3 Verification and Synthesis

The digital circuitry was designed using behavioral Verilog. The behavioral Verilog was then verified using ModelSim (see Figure 4.3) and found to function as desired. The behavioral Verilog was synthesized using X-Fab's standard cell library and Synopsis into a structural file that could be read by Tanner Tools. Tanner Tools then placed the logic cells from the structural file and routed them into the layout shown in Figure 4.4. The digital control module was then wired to the rest of the chip.

By changing the address line that controls which electrode's output is sent to the ADC at a rate that is more than the minimum Nyquist rate, it is possible to transmit signals from 29 electrodes and the three on chip sensors. As the two sensors' output values do not often change, their consistency will help to synchronize the data from the other 29 electrodes once the data is off chip.

Table 4.1. The addresses of the electrodes cycled through in each subset

	The Value of the 3 LSB of the Column Register				
	0	1	2	3	else
Count	Row,Col				
0	0,0	5,0	0,5	5,5	0,0
1	0,1	5,1	0,6	5,6	0,2
2	0,2	5,2	0,7	5,7	0,4
3	0,3	5,3	0,8	5,8	0,6
4	0,4	5,4	0,9	5,9	0,8
5	1,0	6,0	1,5	6,5	2,1
6	1,1	6,1	1,6	6,6	2,3
7	1,2	6,2	1,7	6,7	2,5
8	1,3	6,3	1,8	6,8	2,7
9	1,4	6,4	1,9	6,9	2,9
10	2,0	7,0	2,5	7,5	4,0
11	2,1	7,1	2,6	7,6	5,1
12	2,2	7,2	2,7	7,7	4,2
13	2,3	7,3	2,8	7,8	5,3
14	2,4	7,4	2,9	7,9	4,4
15	3,0	8,0	3,5	8,5	4,6
16	3,1	8,1	3,6	8,6	5,7
17	3,2	8,2	3,7	8,7	4,8
18	3,3	8,3	3,8	8,8	5,9
19	3,4	8,4	3,9	8,9	7,0
20	4,0	9,0	4,5	9,5	7,2
21	4,1	9,1	4,6	9,6	7,4
22	4,2	9,2	4,7	9,7	7,6
23	4,3	9,3	4,8	9,8	7,8
24	4,4	9,4	4,9	9,9	9,1
25	7,2	2,2	7,7	2,7	9,3
26	7,7	2,7	7,2	2,2	9,5
27	5,8	4,8	5,1	4,1	9,7
28	2,7	7,7	2,2	7,2	9,9
29	15,15	15,15	15,15	15,15	15,15
30	14,15	14,15	14,15	14,15	14,15
else	13,15	13,15	13,15	13,15	13,15

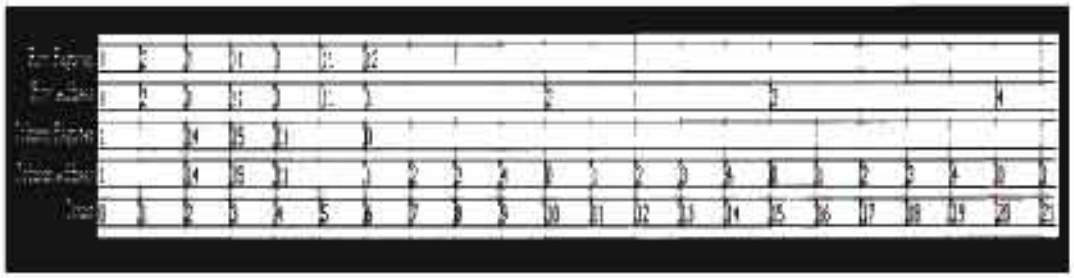

Figure 4.3 ModelSim verification screen shot. Notice that the address buses follow the address registers until the row register is set to 12. At that point the address buses are based upon Table 4.1.

Figure 4.4 The layout of the digital control block.(2051.5 μm $\times$ 148.6 μm)

CHAPTER 5

PROGRAMMING INIE-1

The chip was fabricated using X-Fab's 0.6 μm, 2 poly, 3 metal BiCMOS process. The chip was then packaged in a 64 pin plastic LQFP (Low-profile Quad Flat Package, as seen in Figure 5.1). This chapter begins by explaining what internal signals are accessible from the pins of the package. The correct way to configure the chip for wireless power and operation is then set forth followed by an explanation of the command protocol. The chapter concludes with the command sequence required to program the shift register.

5.1 The Pinout of INI-E1

The way in which the package is connected to the die is shown in Figure 5.2. The pinout diagram for INI-E1 is shown in Figure 5.3. All pins labeled NC (no connect) are not connected internally as verified in Figure 5.2. As such these pins can either be tied to ground or left floating.

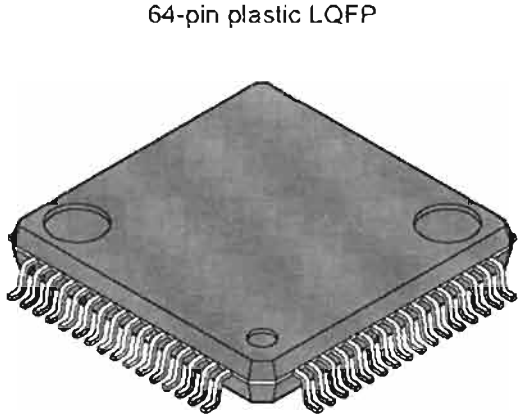

Figure 5.1. The packaging for INI-E1

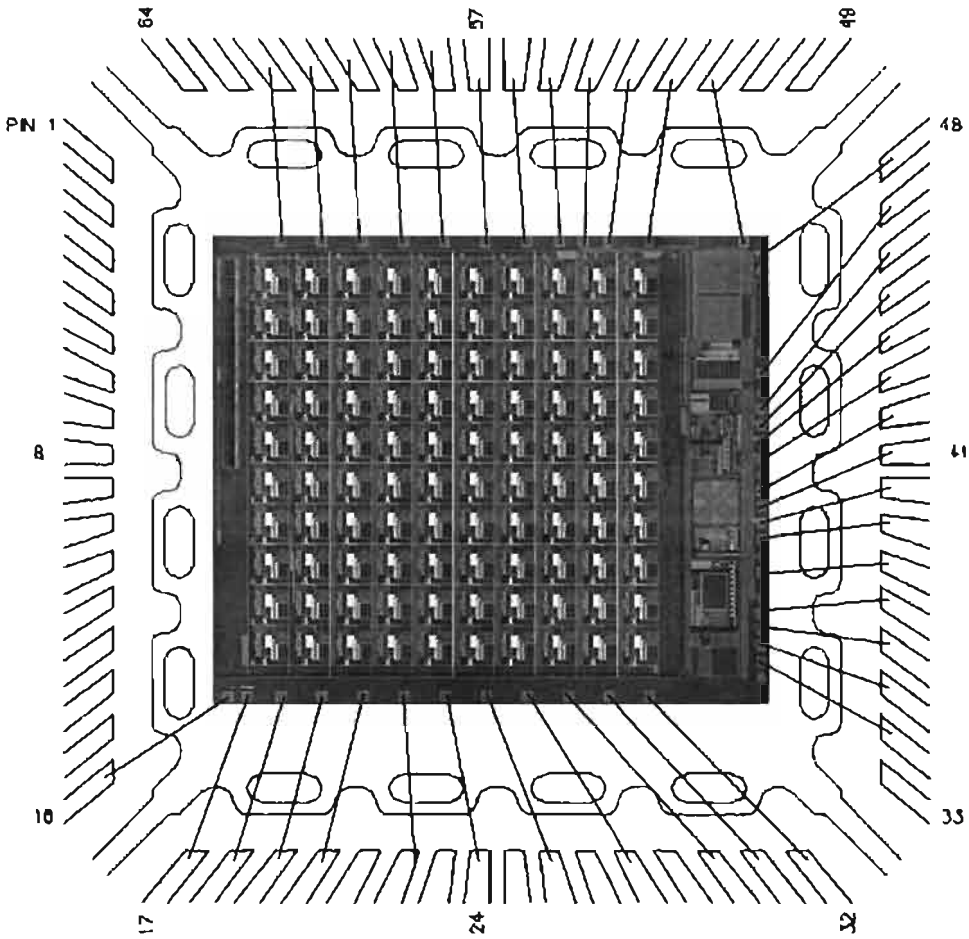

Figure 5.2. The internal pin connections

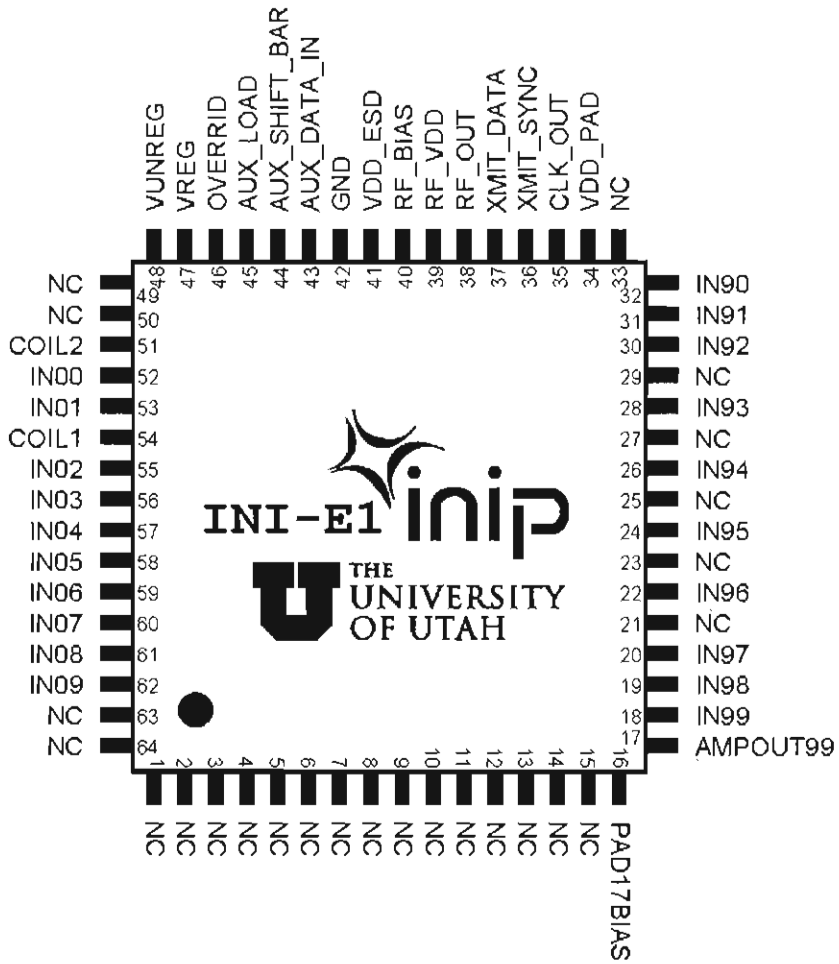

Figure 5.3. The pinout of INI-E1

Twenty electrodes are connected to external pins. These pins are labeled INcr, where c is the column address and r is the row address of the electrode the pin is connected to.

Only one amplifier's output is connected to an external pin. It is the amplifier connected to the electrode with address (9,9). The buffer stage of the amplifier was not designed to drive large external impedances. Therefore, to preserve signal integrity, another buffer is connected to the output of the amplifier. This buffer is connected before the transmission gate to provide continual monitoring of the amplifier's output regardless of which amplifier's output is being sent to the ADC. The buffers driving current is set by a bias circuit that is connected to the pin labeled PAD17BIAS. By placing a 1 MΩ resistor between Pin 16 and ground (GND, Pin 42) enough current will be provided to the pad buffer of Pin 17 so as to drive an oscilloscope.

Pins COIL1, COIL2, VUNREG, and VREG are used to wirelessly power the chip as well as for diagnostics related to power. These pins are explained in the following section. Pins OVERRIDE, AUX_LOAD, AUX_SHIFT_BAR, and AUX_DATA_IN are for sending commands to the chip via wires. Pins RF_VDD, RF_BIAS, and RF_OUT are pins to increase the power of the RF transmitter for an external antenna. Pins CLK_OUT, XMIT_DATA, and XMIT_SYNC are used for diagnosing the telemetry protocols. The pins for sending commands to the chip via wires, increasing the power of the RF transmitter, and diagnostics of the telemetry protocols are not explained in this paper as they were not used. The pin VDD_ESD needs be connected only if these pins are used.

5.2 Configuring the Chip for Wireless Operation

To power INI-E1 a power receiving coil needs to be connected from COIL1 (pin 54) to COIL2 (pin 51). A 10 nF capacitor should be connected from VUNREG (pin 48) to GND (pin 42). The capacitor is one of the two off-chip capacitances needed. The other off-chip capacitor is not always required and is used to set the resonance frequency with the receiving coil [22]. When powered wirelessly the unregulated, rectified voltage can be measured between the pins VUNREG and GND. The voltage should be between 4.0 V and 9.0 V for proper chip operation. To verify the on-chip voltage regulator is maintaining 3 V, the voltage between VREG (pin 47) and GND may be measured.

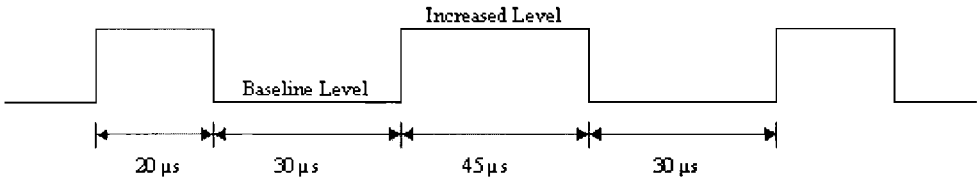

Figure 5.4. The recomended timing diagram for sending '010'

Once powered, INI-E1 will will be operating, but in an unknown state. This is because the control shift register has not yet been set to known values, so all the circuits this register controls are operating under its random start up values. To set the register, commands must be sent via amplitude modulation of the power connection.

5.3 Wireless Command Protocol

To power INI-E1 wirelessly, the inductive link requires a certain amplitude of the voltage across the receiving coil. The voltage level necessary to achieve this is the baseline voltage. Commands are sent to INI-E1 by modulating the amplitude of the inductive power. The amplitude of the power signal is momentarily increased past the minimum level required to power the chip, then decreased back to the baseline power level. When the voltage is set higher than the baseline, a counter on the chip begins to count. Once the counter has finished, the coil voltage level is sampled. If the voltage is still above the baseline then a one is inserted into the shift register. If the voltage has returned to baseline a zero is inserted into the shift register. The counter takes approximately 23 μs. Thus, a pulse longer than 23 μs encodes a one, and a pulse shorter than 23 μs encodes a zero. Each pulse should be followed by at least 25 μs of baseline amplitude before another pulse is sent.

Though this scheme is capable of 20 kbit/s data transmission, to ensure reliable data transfer it is recommended that the minimum timing is not used. The recommended pulse durations are 20 μs high for a zero, and 45 μs high for a one, with an inter-pulse rest period of 30 μs (see Figure 5.4). Following the recommendations, data may be sent at approximately 16 kbit/s. As a complete command sequence contains 1032 bits, using the recommendations to send a command sequence takes approximately 65 ms.

5.4 The Command Sequence for INI-E1

The power transfered through the inductive link is proportional to the voltage across the transmitting coil and inversely proportional to the distance between the transmitting and receiving coil. The plausible accidental temporary shortening of the distance between the power coils creates a strong possibility of a bogus command bit being sent over the inductive link. To prevent bogus commands being accepted by the chip, an eight bit header is required to be sent before bits are actually shifted into the register. Until the correct header bits are sent to the chip, any bit sent, whether accidental or not, will be ignored. The header for INI-E1 is 10101100.

Once the header has been sent, the chip expects to see a command of 1024 bits. Until the chip receives 1024 bits, the bits will not get loaded into the registers. Preceding the shift register is a seven bit shift register which is used to check for the correct header. The seven bit shift register's output is the input to the control shift register. This means that the last 7 bits transmitted to the chip are filler and their content is inconsequential. The control shift register consists of 36 bits. This means that the first 981 bits are filler as well and their content is inconsequential.

The 36 bits in the control shift register control the other on-chip circuits. The first two bits control the depth of the FSK. The next bit enables the FSK. The next eight bits controls the frequency at which the RF transmitter broadcasts. The next five bits control the power at which the RF transmitter broadcasts. The next four bits are the row address, followed by the four bits for the column address. The next 12 bits program the bias generators for the amplifier, first four for stage1, next four for stage2, and the last four for stage3, the buffer.

To 'prime' the analog data acquisition circuits on the chip, a sequence of approximately 50 bits of alternating ones and zeros should be sent before the header. Thus, to send a successful command sequence over the inductive link, send the bits in the following order:

1. 50 alternating ones and zeros to prime the data acquisition.

2. 8 bit header.

3. 981 filler bits whose values are meaningless.
4. 4 bits, with the **most** significant first, that bias the amplifier's buffer.
5. 4 bits, with the **least** significant first, that bias the amplifier's second stage.
6. 4 bits, with the **most** significant first, that bias the amplifier's first stage.
7. 4 bits, with the **most** significant first, for the column address.
8. 4 bits, with the **most** significant first, for the row address.
9. 5 bits, with the **most** significant first, sets the transmission power.
10. 8 bits, with the **most** significant first, sets the transmission frequency.
11. 1 bit that enables the FSK.
12. 2 bits that set the FSK depth.
13. 7 filler bits whose values are meaningless.

This sequence is able to be transmitted in 68 ms. In a recent revision of the chip, the command sequence was shortened from 1024 bits to 64 bits. This shortens the time it takes to send an entire command from 68 ms to 8 ms.

CHAPTER 6

TESTING AND CHARACTERIZATION

Four chips were selected to test and characterize INI-E1. This chapter begins by explaining how these four chips were selected and prepared for testing and characterization. The testing setup and equipment is then explained. The testing and characterization of the amplifier is then discussed, concluded by the testing and characterization of the digital control logic.

6.1 Preliminary Testing and Chip Selection

One hundred fifty seven chips were packaged. Of these, four were used for testing and characterization. As a quick initial testing platform, a socket apparatus was constructed (see Figure 6.1) to test for proper wireless power up and to determine if amplifier (9,9) functioned. Of six randomly selected chips, four of them passed the initial test. These four were then soldered to a printed circuit board (PCB) seen in Figure 6.2. Wires, resistors, and capacitors were then soldered to the PCB and the entire system was placed in a Faraday cage (See Figures 6.3 and 6.4) to shield the circuit from interference. The Faraday cage had connections that allowed BNC cables access to signals, while still shielding the system.

6.2 Wireless Setup and Test Equipment

Once the chips were selected for testing and characterization the following test equipment was used:

- Laptop Computer with Matlab - to control the transmitting coil.
- A National Instrument board (USB 6259) - to interface Matlab and transmitting coil.

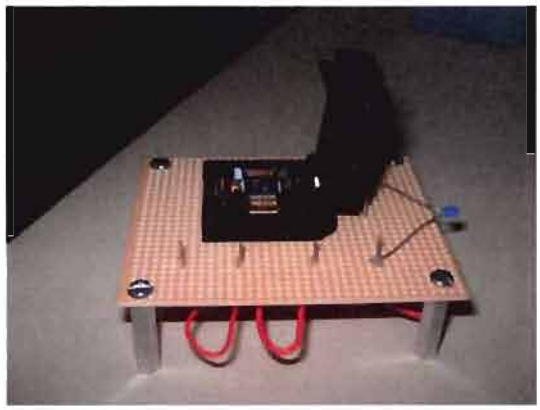

Figure 6.1. The initial testing platform. Chips are easily put into and out of the socket. This allows for the test setup to not be disturbed between chips.

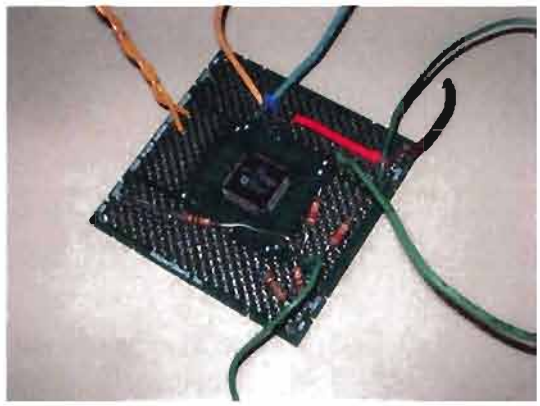

Figure 6.2. One of the four test chips soldered to a PCB.

- Transmitting coil - to wirelessly send commands to, and power, INI-E1.
- Faraday-cage - to shield INI-E1 from noise.
- Tektronix TDS 3054B oscilloscope - to view signals and perform sanity checks.
- Standford Research System SR560 low-noise amplifier - to further amplify signals for high resolution in testing.
- BK Precision 2630 spectrum analyzer - to help locate the frequency at which INI-E1 is broadcasting.

Figure 6.3. The Faraday cage with INI-E1.

Figure 6.4. The Faraday cage closed to shield the circuit during testing.

- Standford Research System SR785 dynamic signal analyzer - to perform frequency-domain analysis of signals.

Excluding the wireless power, the instruments were connected with BNC cables. The typical setup of this equipment can be seen in Figure 6.5.

6.3 Testing and Characterization of the Amplifier

The amplifier was designed for low-noise amplification of the ECoG signals. Thus the transfer function of the amplifiers and the electrode referred noise were tested to see if the design requirements were met. In addition to these tests, it is also important to characterize other aspects of the fabricated amplifier to ensure, that in silicon, the

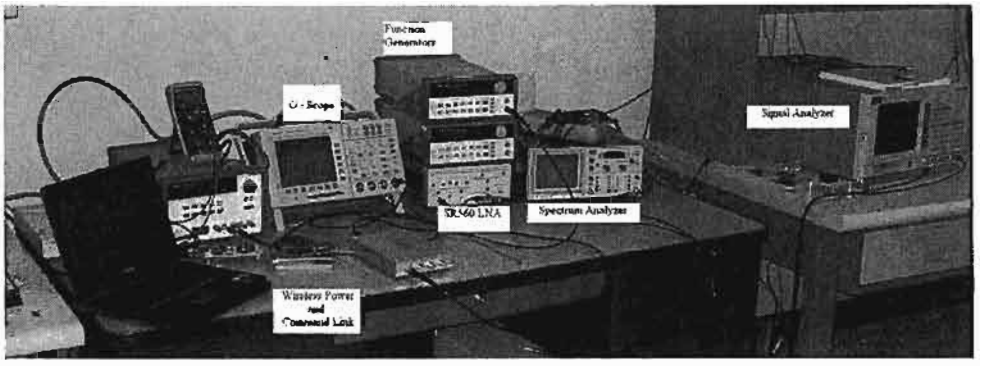

Figure 6.5. The typical setup of the test equipment.

amplifier imeets desired specifications.

6.3.1 Characterization of the Bias Networks and Their Effects on the Amplifier

To control the bandwidth of the amplifiers dynamically, programmable bias networks were designed for each stage. To test the effects the individual networks had on the bandwidth of the entire amplifier, commands were sent to INI-E1 to change the bias of one stage at a time, while the other stages were at full bias. A diagram of the test is shown in Figure 6.6. As the function generators cannot produce an input within the range of ECoG signals the input signal was attenuated by the resistive divider having a gain of -66.8 dB. A 1 V sine wave was than produced by a function generator for input, producing an amplitude of 457 μV at the amplifier input. The bandwidth of the amplifier was then acquired by increasing the frequency of the wave and measuring the output voltage on the scope until the gain was 3 dB below the midband gain. The results of the test are displayed in Table 6.1.

It is interesting to note that with the minimum possible bias current for the buffer (stage3), that the bandwidth is not affected. To conserve power, while maintaining a high frequency cut off 200 Hz, the bias stage registers for stages one, two, and three, may be set to 14, 14, 0, respectively.

6.3.2 The Tested Transfer Function

To find the transfer function of the amplifier, the setup in Figure 6.6 was modified so that the signal analyzer was driving the input and looking at the output of the SR560

Table 6.1. The effects of the bias generators on the bandwidth of the amplifier. (Note: only one stages bias is changed at a time. While one stage is being tested the other stages are at maximum bias.)

Stage Bias Register Value	High frequency cut off in Hz, due to: Stage1	Stage2	Stage3
0	99	79	240
1	103	83	240
2	110	88	240
3	112	91	240
4	120	96	240
5	128	102	240
6	134	106	240
7	142	115	240
8	150	125	240
9	160	135	240
10	170	145	240
11	180	155	240
12	200	175	240
13	210	200	240
14	230	210	240
15	240	240	240

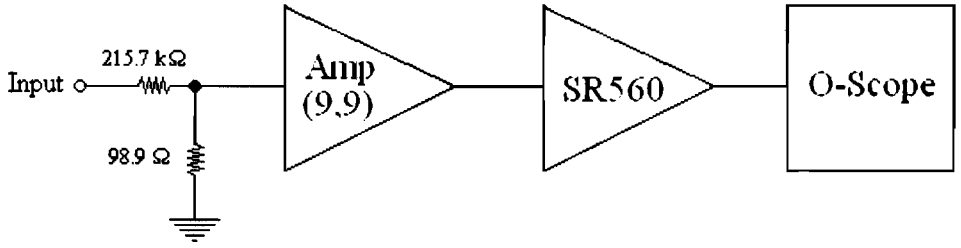

Figure 6.6. The system diagram to test the bias networks

LNA. The signal analyzer was used to find the magnitude of the transfer function of all four test chips, as seen in Figure 6.7. For this experiment the bias networks were all set to their maximum bias. At this bias rate the amplifiers exceed the specification to have a high cut-off frequency of at least 200 Hz. It is also seen from Figure 6.7 that the low frequency cut-off specification is met and is much less than 0.1 Hz.

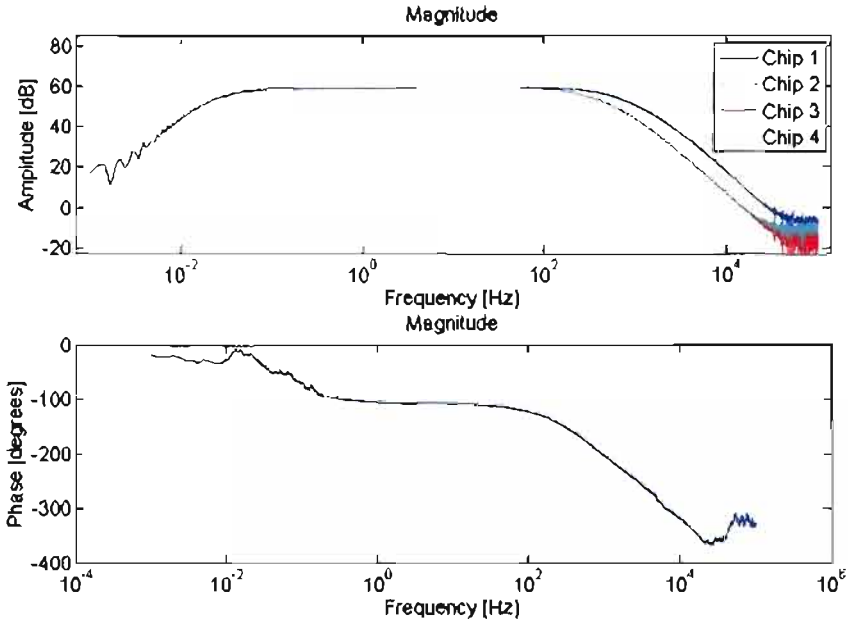

Figure 6.7. The amplifiers bode plot. Magnitude of all four test chips, and the phase of one.

6.3.3 The Electrode Cross Talk

When a signal is applied to one electrode, a nearby electrode can receive the same signal, although degraded, due to capacitive or inductive coupling. This phenomenon is called cross talk. To test the cross talk between electrodes the circuit was connected as shown in Figure 6.8. The spectrum analyzer would drive an electrode. The electrode, directly adjacent to the one being driven, was grounded and its amplifier's output was analyzed. The electrode to electrode cross talk (Figure 6.9) is given by:

$$CrossTalk = \frac{V_o/A_T}{V_i} \tag{6.1}$$

where V_o is the output of the amplifier, A_T is the gain of the amplifiers, and V_i is the input into amplifier (9,8). The in band (less than 200 Hz) cross talk is approximately -45 dB. As ECoG signals have a maximum amplitude of 1 mV this means that the maximum signal seen on an electrode due to cross-talk is less than 6 μV. This amount of cross talk is inconsequential as the maximum cross talk is slightly higher than the electrode referred

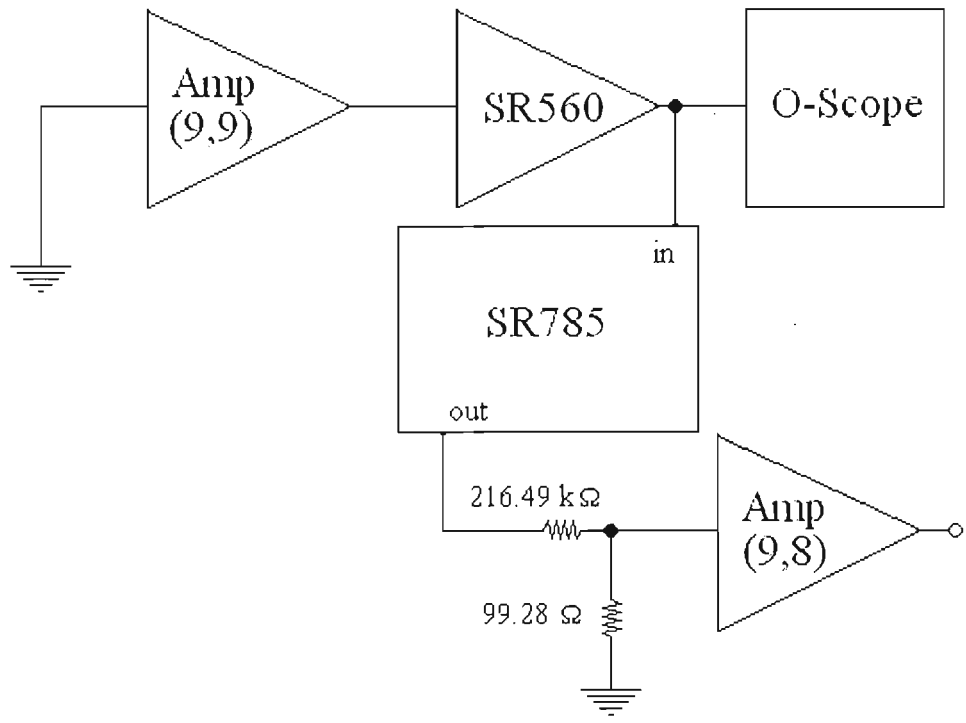

Figure 6.8. The system to measure the cross talk

noise-floor (discussed in section 6.3.5) and 10 times less than that of the minimum ECoG signal need to be recorded.

6.3.4 Power Supply Rejection Ratio of the Amplifier

To find the power supply rejection ratio (PSRR) of the amplifier, the chip was initially powered up wirelessly. Commands were then sent to the chip. Then the signal analyzer was connected to the chips regulated voltage, at which time the wireless power was then turned off and the schematic shown in Figure 6.10 was realized. The signal analyzer generated a sine wave of 141.4 mV (1 mV_{rms}) with an offset of 3.1 V to power the chip. The PSRR was than found according to:

$$\frac{1}{PSRR} = \frac{V_o}{V_i}\frac{1}{A_T} \tag{6.2}$$

where V_o is the output of the LNA, A_T is the gain of the amplifier and LNA, and V_i is the input into amplifier's power. The result is Figure 6.11.

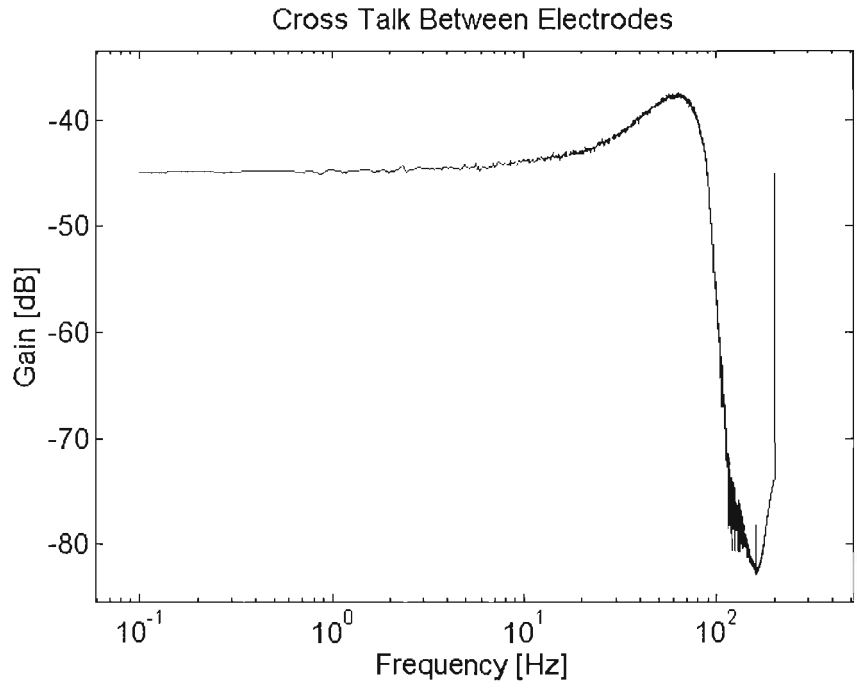

Figure 6.9. The magnitude of the cross talk between electrodes

As the unregulated power supply is more likely to vary due to the nature of the wireless power, it was prudent to measure the PSRR of the amplifier with respect to variation in the unregulated power supply. This was more difficult than the measurement of the regulated voltage, as the signal analyzer can not produce the high offset needed for the unregulated power. The solution was continue to have the chip powered by the wireless connection but use a 1 mF capacitor to couple the unregulated voltage to the signal analyzer, as shown in Figure 6.12. The PSRR is shown in Figure 6.13, again using the definition of PSRR from equation (6.2).

6.3.5 Electrode Referred Noise

The total noise generated by the amplifier was found by connecting the circuit shown in Figure 6.14. The signal analyzer was then used to find the spectral density of the noise. By dividing by the gain of the amplifier and LNA, to input refer the noise, the spectral density was then integrated to find the total electrode referred noise (Figure 6.15).

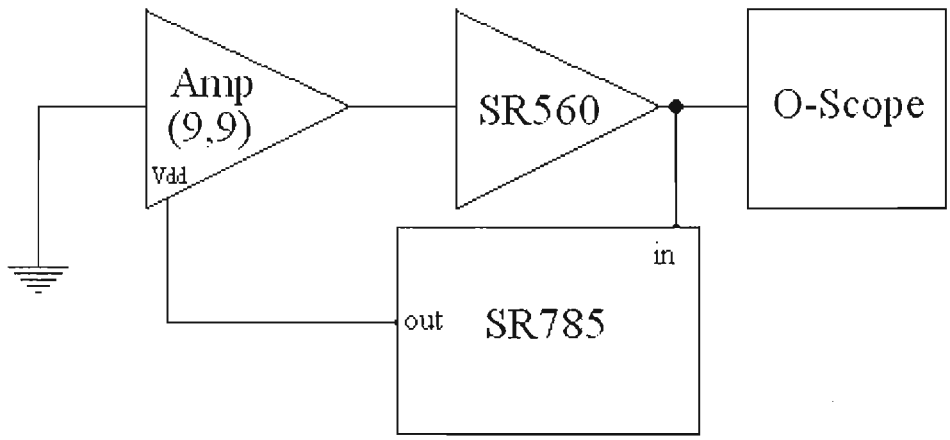

Figure 6.10. The schematic to find the PSRR of the amplifier

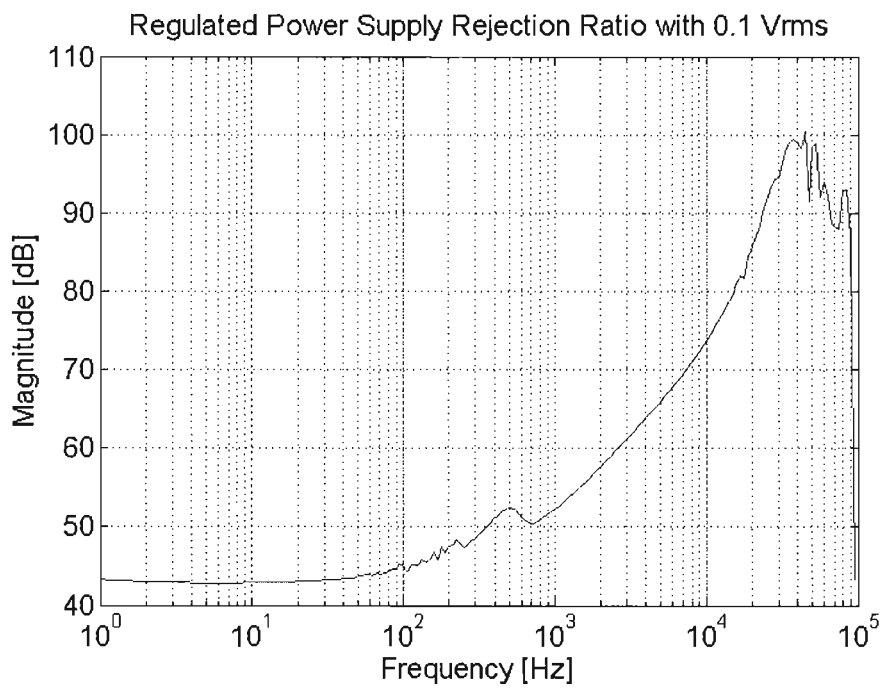

Figure 6.11. The PSRR of the amplifier

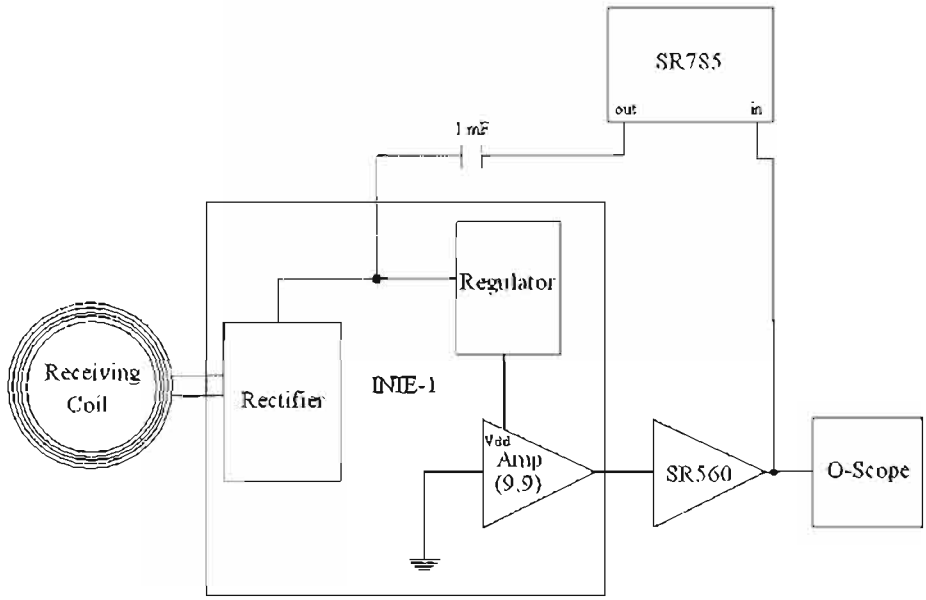

Figure 6.12. The schematic to find the unregulated PSRR

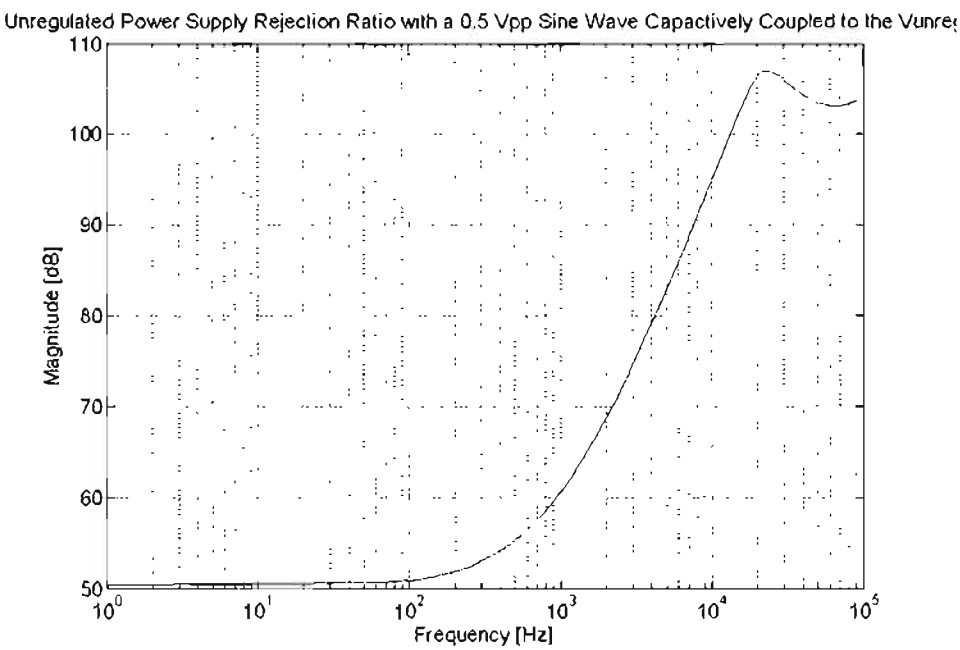

Figure 6.13. The PSRR of the unregulated power. The transfer function of the coupling capacitor is taken into account.

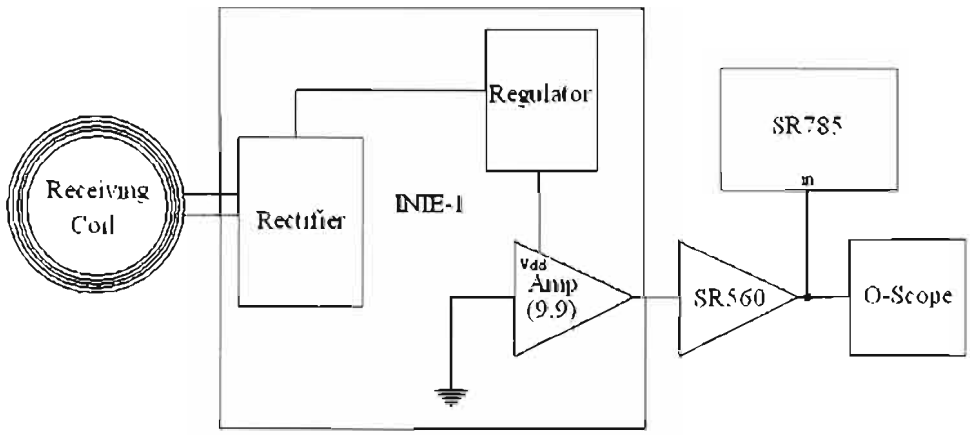

Figure 6.14. System to find the total electrode referred noise

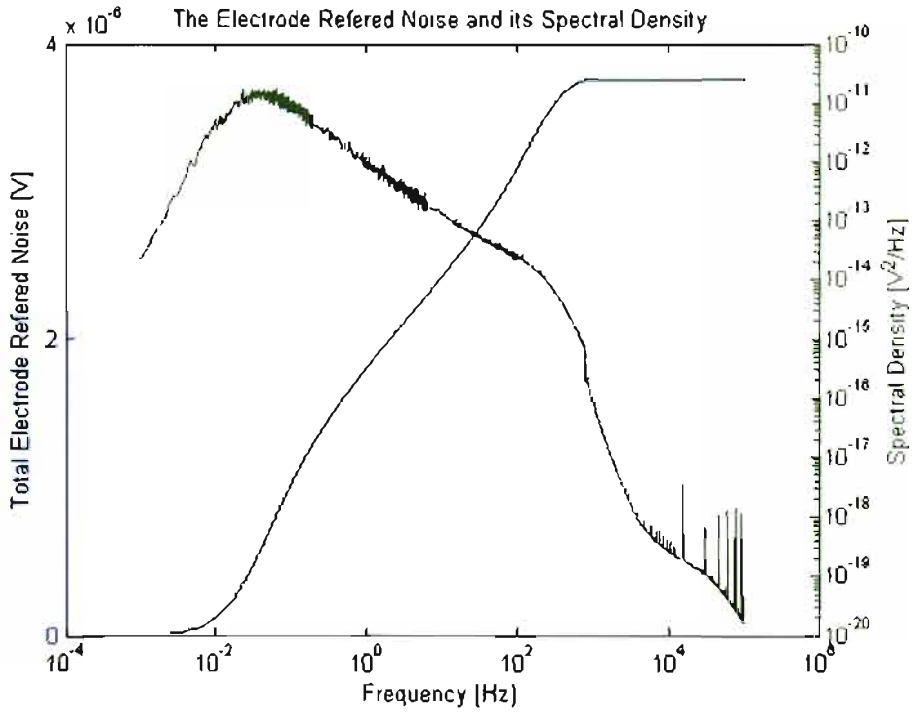

Figure 6.15. The total electrode referred noise

The total electrode-referred noise is 3.5 μV_{rms}, which meets the specification. However some of this noise is due to finite PSRR. To calculate how much noise is present at the electrode due to finite PSRR, the noise on the regulated power was measured using the setup shown in Figure 6.16. Using the same process to find the total noise, the noise of the regulated power (Figure 6.17) is found to be 260 μV. Using the in-band PSRR of 42 dB to refer the noise due to PSRR to the electrode, we find that the electrode-referred noise of the regulated voltage is 2.1 μV_{rms}. The total electrode referred noise, V_{n_tot}, is a function of the amplifier noise, V_{n_amp}, and the noise generated by the PSRR, V_{n_psrr}, and is given by:

$$V_{n\_tot} = \sqrt{V_{n\_amp}{}^2 + V_{n\_psrr}{}^2} \tag{6.3}$$

Thus then implies that the electrode referred noise generated by the amplifier is 2.8 μV_{rms}.

6.4 Testing of the Digital Control

As there is only one amplifier whose output is connected to a pin, the only way to test the digital control logic was to wirelessly receive and decode the transmission of the data from INI-E1. The instrument shown in Figure 6.18 receives the signal from INI-E1 and exports the received data via a digital-to-analog converter (DAC).

To test the digital control logic, a sine wave of 10 Hz was applied to electrode (9,8) and

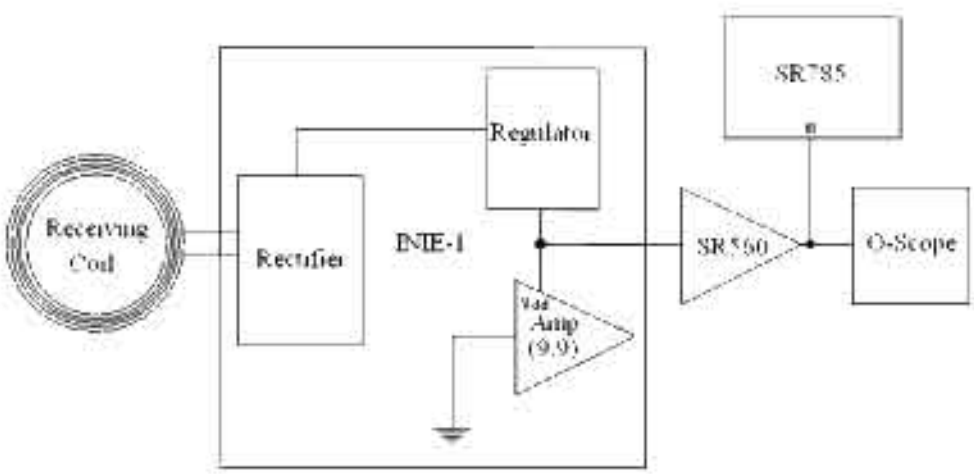

Figure 6.16. System to find the noise of the regulated voltage

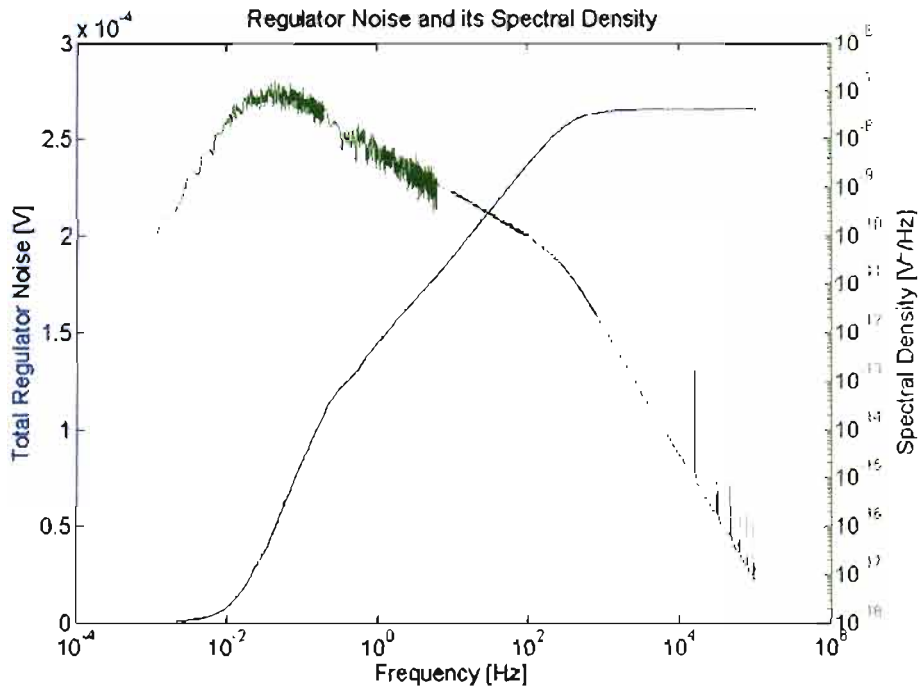

Figure 6.17. The noise of the regulated voltage (not electrode referred)

a triangle wave of 60 Hz was applied to electrode (9,9). The address registers were then programed to cycle through the pattern that included both these electrodes. The receiver's ADC output was connected to the oscilloscope. The data were then captured from the oscilloscope and loaded into Matlab. A program was written to find which samples from the oscilloscope were attributed to each of the 32 signals. Figure 6.19 shows the samples of the oscilloscope as black diamonds. The red and green lines connect the samples that correspond to electrodes (9,9) and (9,8) respectively. This shows that digital control logic is working and capable of transmitting the data from multiple electrodes.

Figure 6.18. Picture of the RF reciever. The DAC's output is the bottom right BNC connector.

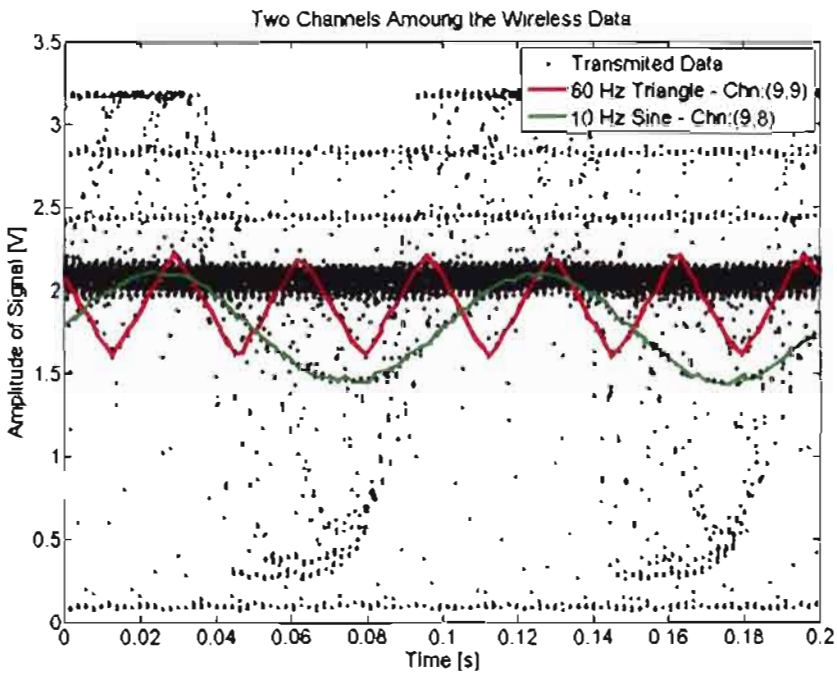

Figure 6.19. The wireless data

CHAPTER 7

CONCLUSIONS

The goal of this project was to design an integrated circuit that could record electrocorticograms. The chip also needed to have circuitry that would allow it to be powered wirelessly and communicate wirelessly. This goal was achieved in the IC called integrated neural interface electrocorticogram recorder (INI-E1) (see Figure 7.1). INI-E1 is able to rectify and regulate power through an inductive link. It is also able to receive commands wirelessly through the power link. The chip is able to record from 100 electrodes. It is able to wirelessly transmit, with 10 bits of accuracy, the amplified signals from the electrodes. It has the capability of transmitting either a single electrode's signal at a time, or transmitting 29 different electrodes' signals in multiplexed fashion.

The project is an extension of past research on the integrated neural interface project. As such, the solutions for wireless power and transmission of data had already been proven. The scope of this project was to design a low power, low noise, amplifier for the amplification of the electrocorticograms, and control logic to enable the continual transmission of data from 29 different electrodes.

The design of the low power, low noise, amplifier was a success; meeting or exceeding every specification summarized in Table 7.1. The characterization of the fabricated amplifier exceeded the required specifications and included power supply rejection ratio (see Section 6.3.4) and cross talk (see Section 6.3.3). The cross talk of the electrodes was found to be inconsequential to the circuit as the maximum cross talk of 6 μV is on the same order of magnitude as the 3.5 μV of total electrode referred noise floor. Due to limitations of testing the chip, the power dissipated from an individual amplifier could not be determined. However, simulation results show that the amplifier is well within its power budget.

Table 7.1. Realization of the specifications for the amplifier

Electrical Atribute	Specification	Measured Result
Low Cut-off Frequency	$\leq$ 0.1 Hz	0.05 Hz
High Cut-off Frequency	$\geq$ 200 Hz (programmable)	79 – 240 Hz
Gain	60 dB	59.2 dB
Power Consumption	$\leq 20\ \mu W$	4.5 μW (simulated)
Layout Area	$\leq$ 46,500 μm^2	46,500 μm^2
Input Referred Noise	$\leq 5\ \mu V_{rms}$	2.8 μV_{rms}

As there seems to be no published integrated amplifiers devoted solely to the purpose of amplifying ECoG signals, a comparison to INI-E1's amplifier can be made only to an amplifier that has the functionality of amplifying a diversity of neural signals, with a design emphasis to include ECoG. The amplifier compared to INI-E1 exceeds the design of INI-E1 in some respects but does not meet all the requirements as set out in Table 3.1. Table 7.2 summarizes this comparison with an amplifier designed in [1].

The design of the control logic was also successful. After INI-E1 was programmed to the mode of continuously broadcasting the data recorded from 29 electrodes, a wireless receiver was used to receive the data, convert it, and display it on an oscilloscope. It was found that the data from individual electrodes could be recovered.

Although INI-E1 fulfilled its design requirements, perhaps the biggest limitation is the number of electrodes that it can wirelessly transmit data from continuously. As shown in a recently published paper [23], the spatial resolution of ECoG signals is smaller than thought, thus necessitating the need for data from more electrodes. As the amplifier uses significantly less power than anticipated, it would be advantageous to use the power saved in the amplifier to increase the sampling speed of the ADC. This would allow for more electrodes amplified signals to be sampled within the Nyquist rate and increase the amount of electrodes that could be continuously transmitted off chip.

The design of the amplifier and control logic in the development of the integrated circuit, INI-E1, will allow neuro-scientist to discover more about the brain and develop more applications for recording brain signals. It is hoped that the work done in this thesis will help researchers improve lives through the use of wireless brain machine interfaces.

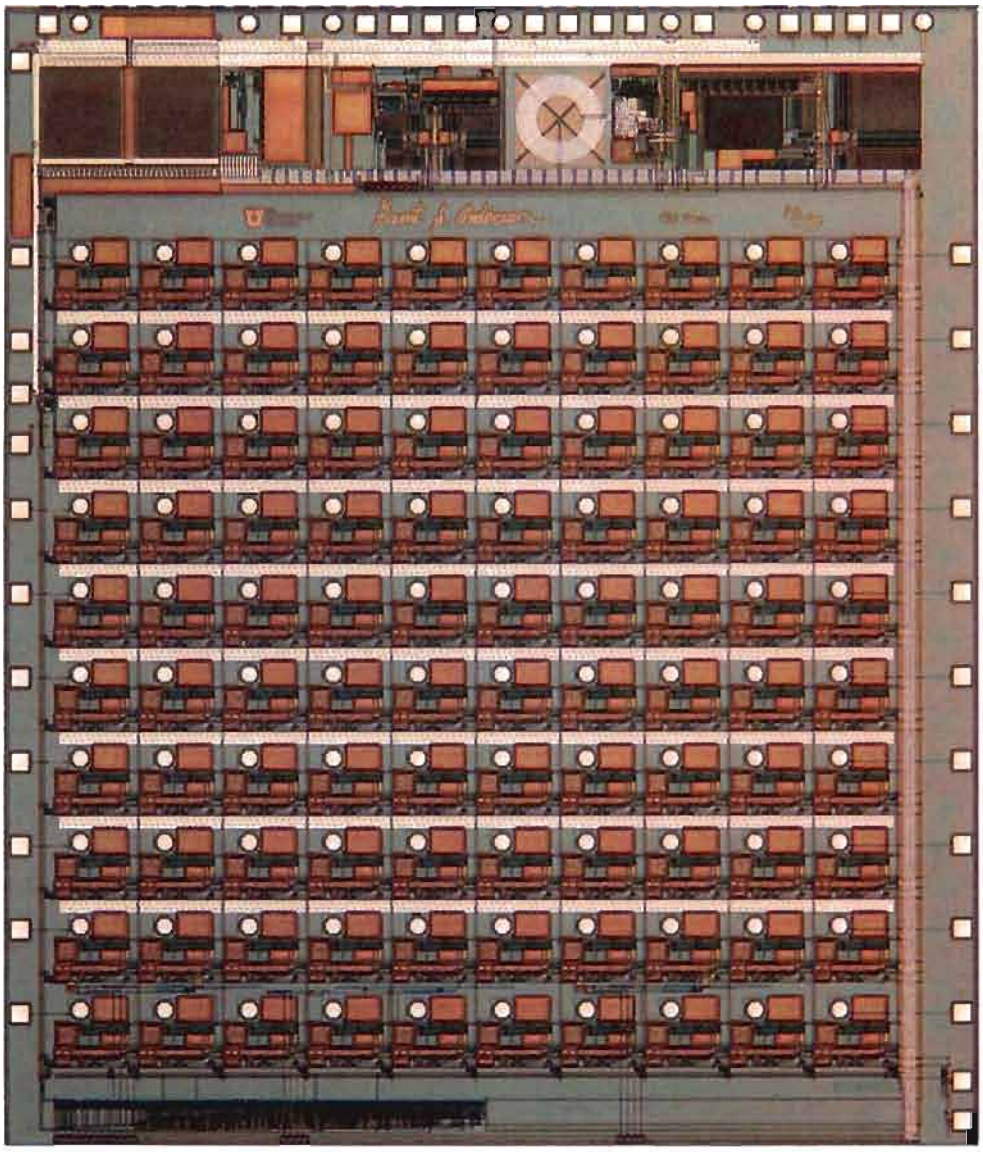

Figure 7.1. The fabricated INI-E1 (4,675 μm × 5,365 μm)

Table 7.2. Comparison of the amplifier for INI-E1 and the amplifier found in [1]

Specification	INI-E1	Amplifier [1]
Low Cut-off Frequency	0.05 Hz	0.2 Hz
High Cut-off Frequency	200 Hz	140 Hz
Gain	59.2 dB	39.6 dB
Power Consumption	4.5 μW	1 μW
Input Referred Noise	2.8 μV_{rms}	1.65 μV_{rms}

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